EE 143 **FINAL EXAM** **NAME** ________________________

C. Nguyen **May 10, 2010**

INSTRUCTIONS

- Read all of the instructions and all of the questions before beginning the exam.
- There are 5 problems on this Final Exam, totaling 143 points. The tentative credit for each part is given to help you allocate your time accordingly. You have a total of 3 hours to finish this exam. Be careful not to spend all your time on any one part.
- This is a closed book exam, except you can have two two-sided 8.5″×11″ sheet of notes and a calculator.
- Unless otherwise noted on a particular problem, you must show your work (in the space provided plus the backs of the pages, if needed) for all problems to receive full credit; *simply providing answers will result in only partial or no credit, even if the answers are correct*. If you require extra space beyond what is provided, be sure to turn in any material that is required to support your solutions. Note that there are extra pages at the end of this exam. Do not use any attached pages until you have exhausted the pages contained in this exam.
- Turn in the entire exam, including this cover sheet.
- Put your name on every page of this exam, as well as on any additional material that you submit.
- Be sure to provide units where necessary.

Signature: ____

Problem 1:	/ 38 points
Problem 2:	/ 25 points
Problem 3:	/ 20 points
Problem 4:	/ 25 points
Problem 5:	/ 35 points
Total:	/ 143 points

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Problem 1. **Total 38 points**

Please provide short written answers to the questions that follow.

(a) Which technology was the first in volume production, NMOS or PMOS, and why?

(b) Are substrate doping levels higher or lower in modern (i.e., today's) CMOS versus 1990's CMOS? Why?

(c) A silicon wafer is uniformly doped with boron (to $2x10^{15}$ cm^{-3}) and phosphorus (to $1x10^{15}$ cm^{-3}) so that it is net p-type. This wafer is then thermally oxidized to grow about 1 μm of SiO_2. The oxide is then stripped and a measurement is made to determine the doping type of the wafer surface. Surprisingly it is found to be n-type. Explain why the surface was converted from p- to n-type.

Problem 1. (continued)

(d) To etch aluminum, you use a solution composed of:

80% phosphoric acid (H_2PO_4) + 5% nitric acid (HNO_3)

+ 5% acetic acid (CH_3COOH) + 10% water (H_2O)

i) Explain the mechanism by which the above solution etches aluminum.
ii) What is the biggest problem with use of this solution and how might you best solve it?

(e) How does chemical mechanical polishing (CMP) differ from lapping?

(f) Suppose you ran a CMOS process up to metal patterning and tested your devices before finishing the entire process just to see if the devices were functional. Suppose this test reveals that all of your threshold voltages are wrong. What should you do to fix this and how does your solution work?

<u>Problem 1</u>. (continued)

(g) In LOCOS oxidation, patterned films of nitride on oxide are used to block oxidation over active area regions. Unfortunately, LOCOS also introduces "bird's beaks" that encroach into the active regions, and this limits how small an MOS device can be made. Can we suppress the bird's beak in LOCOS by dispensing with the oxide film and instead depositing nitride directly over silicon? What would be the problem with this approach? Explain.

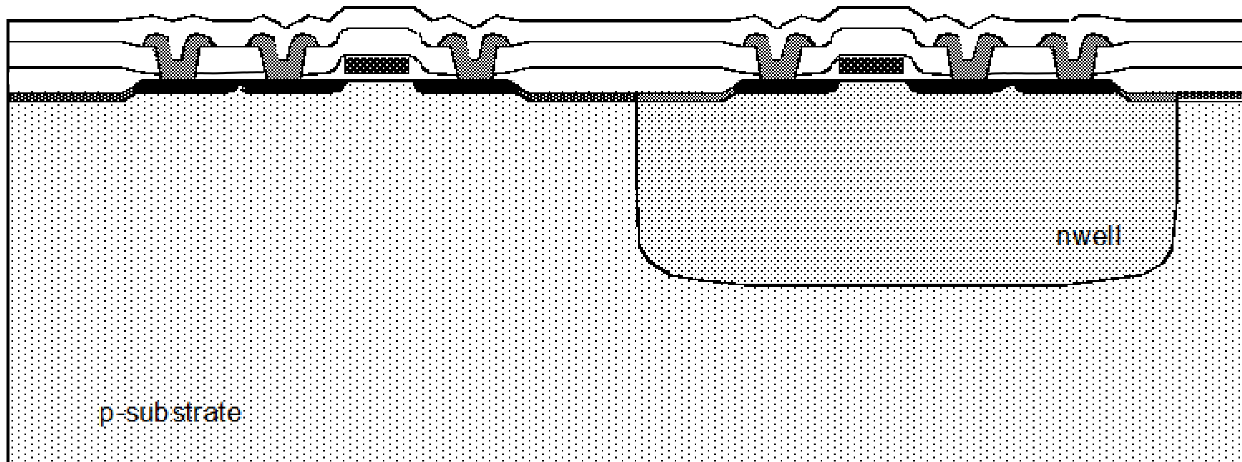
(h) Suppose you plan to use a stepper projection lithography tool to pattern polysilicon over oxide. The tool uses an exposure wavelength of 200 nm and has a numerical aperture of 0.5. What is the minimum theoretical feature size that this tool can resolve? What is the maximum height of topography over the wafer surface that this tool can handle while maintaining this resolution?

Problem 2. **Total 25 points**

The cross-section for a standard, LOCOS-isolated, **nwell** CMOS technology (similar to the pwell process described in lecture) is shown below.

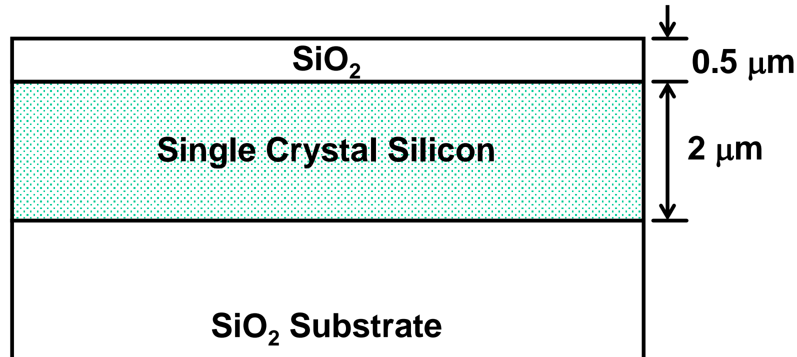
(a) Label all layers in the process, including n+ and p+ diffusions. Also, delineate thermal oxides from LPCVD oxides. Then use wires (i.e., lines) and batteries to implement an inverter in this technology, hooking up relevant portions to V_{DD} and ground, and clearly indicating inputs and outputs.

(b) Draw on the figure the cross-section of a guard ring at a location that provides the most effective protection against latch-up. Indicate the dopant type used and the bias voltage to which this ring is attached. Explain why this location is better than any other. Draw parasitic transistors and current direction arrows to aid in your explanation



Problem 3. **Total 20 points**

Boron ions are implanted into the SiO_2-Silicon-SiO_2 sandwich structure shown below at a dose of 10^{15} cm^{-2}. A subsequent high temperature step at 1000°C for 4 hrs in a N_2 ambient is used to activate and drive-in the dopants. To simplify the problem, you can assume that the diffusion coefficient D_{boron} (=7.2×10^{-3} μm^2/hr at 1000°C) is the same in Si and SiO_2, that there is no boron segregation at the Si-SiO_2 interface, and that that implanted ranges of B^+ in silicon and SiO_2 are the same.



(a) What is the implant energy that achieves the lowest possible sheet resistance in the silicon layer?

(b) Estimate the sheet resistance.

More work space next page.

<u>Problem 3</u>. (continued)

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Problem 4. Total 25 points

The drain currents for four NMOSFETs on the same die with the same W_{drawn}'s (=50μm), but with different L_{drawn}'s, were measured for two different V_{GS}'s, with drain voltages set at 50mV, and sources and bulks tied to ground. The resulting data are summarized as follows:

L_{drawn} [μm]	2	4	6	8
I_d (V_{GS} = 3V) [μA]	16	6.9	4.5	3.3
I_d (V_{GS} = 6V) [μA]	28	12.7	8.2	6.0

For this problem, assume that the effective channel width $W_{eff} = W_{drawn}$, the threshold voltage V_t = 0.7V, and the gate oxide thickness X_{ox} = 20nm, for all devices. Also assume that for a device with no external series resistance R_{ext}, the drain current I_d in the linear region (i.e., with small V_{DS}) is given approximately by

$$I_d = \frac{\mu_o}{1+\theta(V_{GS}-V_t)}\frac{W_{eff}}{L_{eff}}C_{ox}(V_{GS}-V_t)V_{DS}$$

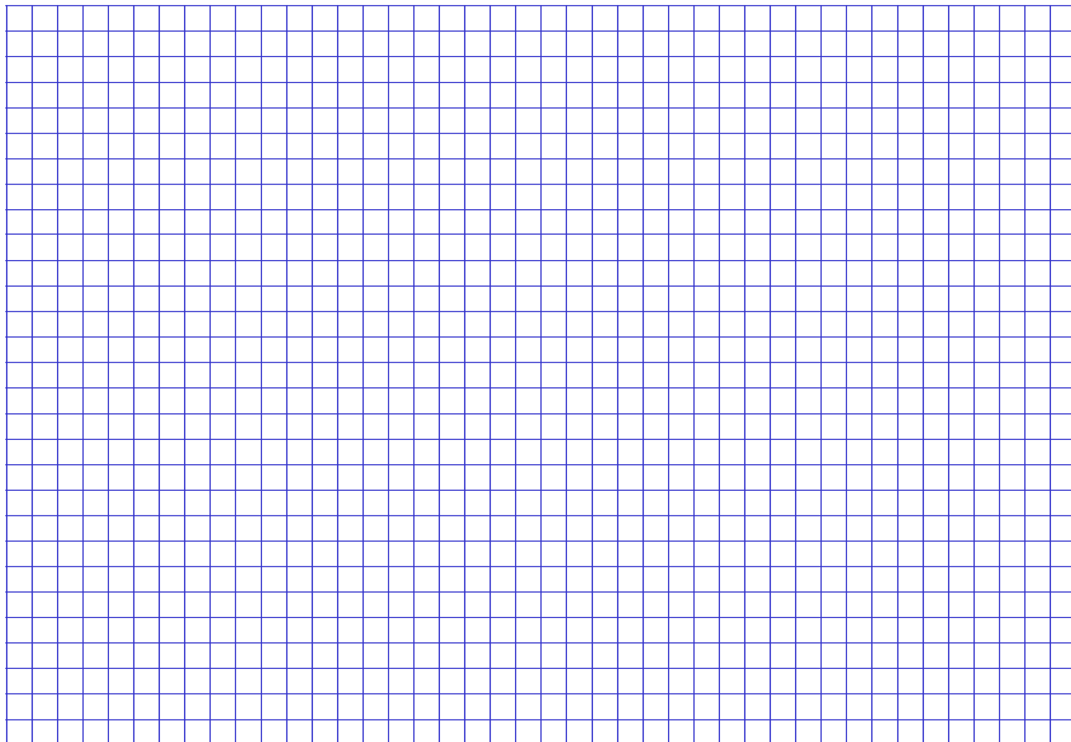
Use the data and the graph paper below to determine the following parameters:

(a) the external resistance in series with the channel, R_{ext}

(b) $\Delta L = L_{drawn} - L_{eff}$, where L_{eff} is the effective channel length considering all sources of deviation

(c) the low field mobility, μ_o; and

(d) θ of the devices.



Problem 4. (continued)

More work space next page.

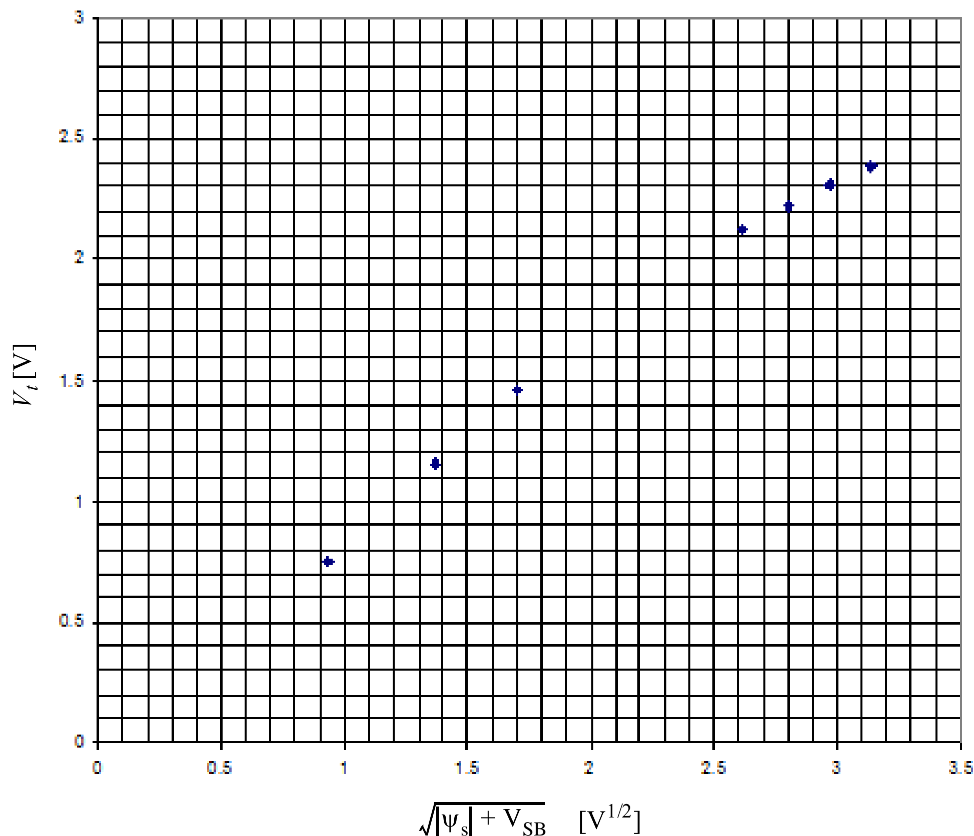
Problem 4. (continued)

Problem 5. **Total 35 points**

The simplified CMOS process flow used to fabricate an NMOS transistor is as follows:

i) CMOS twin-well processing steps to form nwell's and pwell's, both with doping N_{sub}=??? cm^{-3}, and standard LOCOS to define active areas.
ii) Sacrificial oxide growth: Target = 30 nm, 900°C, 20 min. dry O_2.
iii) Threshold implant: B11, E = 10 keV, D_I =???cm^{-2}.
iv) Strip sacrificial oxide.
v) Gate oxidation: 900°C, 12 min. dry O_2 + 20 min. N_2 anneal. Target = 10 nm.
vi) Polysilicon gate deposition: 650°C, 1 hr. 35 min. Target = 250 nm.
vii) Gate definition.
viii) Re-oxidation: 900°C, 14 min. dry O_2 + 10 min. N_2 anneal. Target = 20 nm SiO_2 on poly.
ix) n+ S/D implant and anneal: 925°C, 20 min. in N_2.
x) p+ S/D implant.
xi) PSG deposition: 450°C. Target = 300 nm.
xii) PSG densification: 925°C, 20 min. wet O_2.
xiii) Contact hole mask.
xiv) Metal deposition, masking, and patterning.
xv) Low temperature sintering.

After fabricating an NMOS device using the above process flow, measurements are taken on the device to yield a plot of threshold voltage V_t versus the square root of the inversion surface potential magnitude $|\psi_s|$ plus V_{SB} as shown below.



Problem 5. (continued)

In this problem, when calculating threshold voltages or determining effective dopant depths, use the approximation $N_s x_s = Q$, where Q is the effective implanted dose in the silicon, and x_s is the effective depth of the implanted profile, assumed to have a constant dopant concentration of $N_{tot} = N_s \pm N_{sub}$. (Do not assume that N_s=0.5N_o; rather, determine N_s (or N_{tot}) from the experimental data.)

Finally, assume that as an oxide grows over silicon, dopant atoms in the path of the oxide front end up in the oxide; those that are not reached by the oxide stay in the silicon.

Answer the following questions.

(a) Determine the effective depth of the threshold implant, x_s.

(b) Determine the threshold implant dose D_I used in the above process.

(c) Determine the background substrate concentration, N_{sub}.

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Problem 5. (continued)

More work space next page.

Problem 5. (continued)

Extra Page.

Possibly Useful Data:

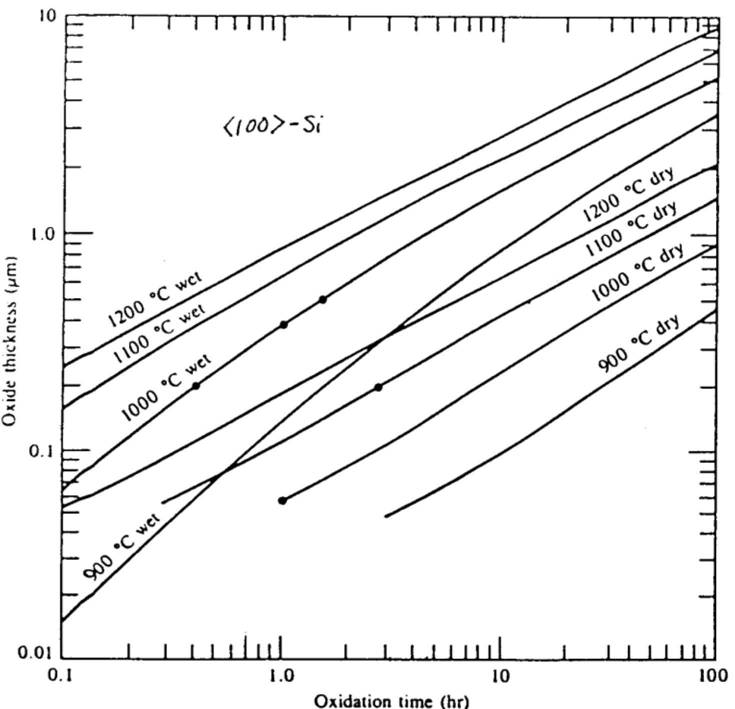

Table 4.1 Typical Diffusion Coefficient Values for a Number of Impurities.

Element	D_0(cm^2/sec)	E_A(eV)
B	10.5	3.69
Al	8.00	3.47
Ga	3.60	3.51
In	16.5	3.90
P	10.5	3.69
As	0.32	3.56
Sb	5.60	3.95

LSS RANGE STATISTICS FOR

BORON IN SILICON

SUBSTRATE PARAMETERS

SILICON

Z 14

M 28.090

N 0.4995E 23

RHO/R 0.3190E 02

EPS/E 0.1130E 00

CNSE 0.3242E 02

MU 2.554

GAMMA 0.8089

SNO 0.9211E 02

ION: BORON

Z 5

M 11.000

ELECTRONIC CROSS SECTIONS OF EISEN

NORTHCLIFFE CONSTANT 0.252E 04

ENERGY (KEV)	PROJECTED RANGE (MICRONS)	PROJECTED STANDARD DEVIATION (MICRONS)
10	0.0333	0.0171
20	0.0662	0.0283
30	0.0987	0.0371
40	0.1302	0.0443
50	0.1608	0.0504
60	0.1903	0.0556
70	0.2188	0.0601
80	0.2465	0.0641
90	0.2733	0.0677
100	0.2994	0.0710
110	0.3248	0.0739
120	0.3496	0.0765
130	0.3737	0.0790
140	0.3974	0.0813
150	0.4205	0.0834
160	0.4432	0.0854
170	0.4654	0.0872
180	0.4872	0.0890
190	0.5086	0.0906
200	0.5297	0.0921
220	0.5706	0.0950
240	0.6108	0.0975
260	0.6496	0.0999
280	0.6875	0.1020
300	0.7245	0.1040
320	0.7607	0.1059
340	0.7962	0.1076
360	0.8309	0.1092
380	0.8651	0.1107
400	0.8987	0.1121
420	0.9317	0.1134
440	0.9642	0.1147
460	0.9963	0.1159
480	1.0280	0.1171
500	1.0592	0.1182
550	1.1356	0.1207
600	1.2100	0.1230
650	1.2826	0.1252
700	1.3537	0.1271
750	1.4233	0.1289
800	1.4917	0.1306
850	1.5591	0.1322
900	1.6254	0.1337
950	1.6905	0.1351
1000	1.7556	0.1364

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LSS RANGE STATISTICS FOR

PHOSPHORUS IN SILICON

SUBSTRATE PARAMETERS

SILICON

Z 14

M 28.086

N 0.4995E 23

RHO/R 0.2889E 02

EPS/E 0.2137E-01

CNSE 0.2449E 02

MU 0.907

GAMMA 0.9976

P 0.53

SNO 0.4413E 03

ION: PHOSPHORUS

Z 15

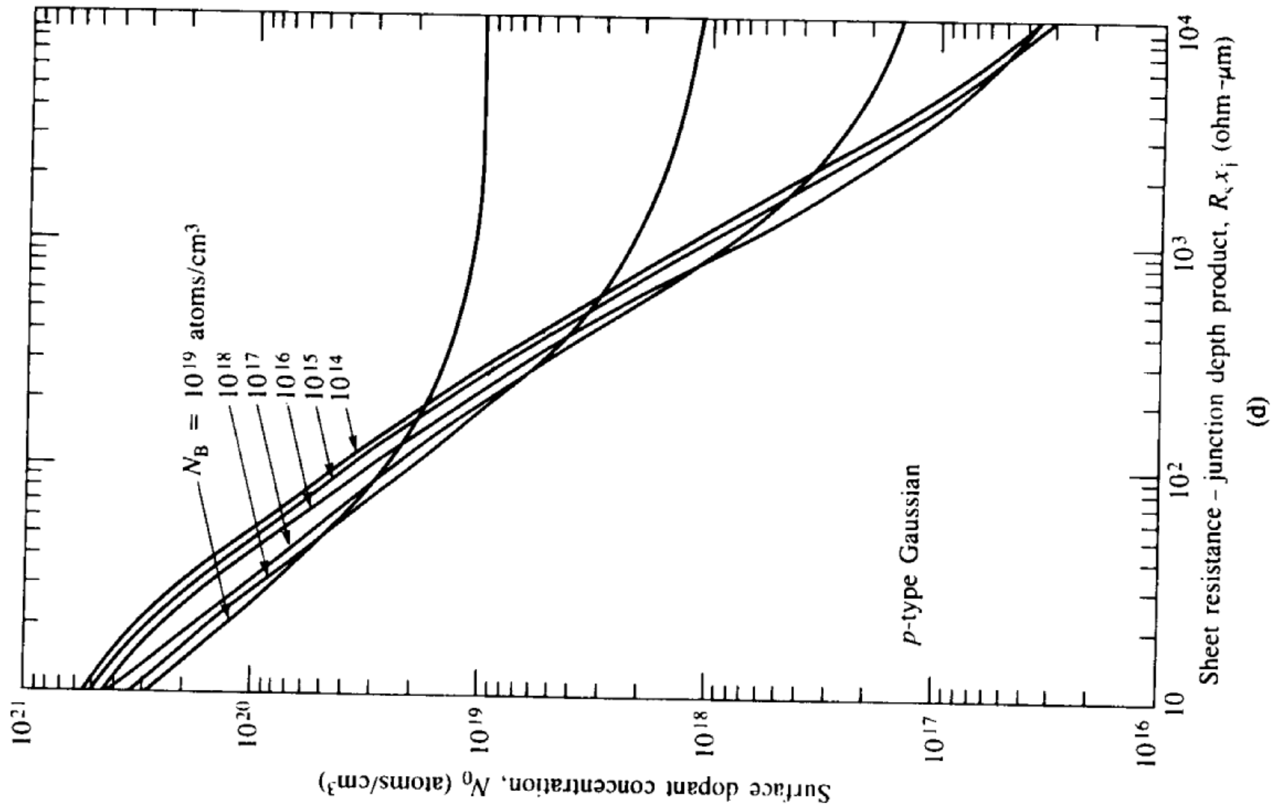
M 30.974

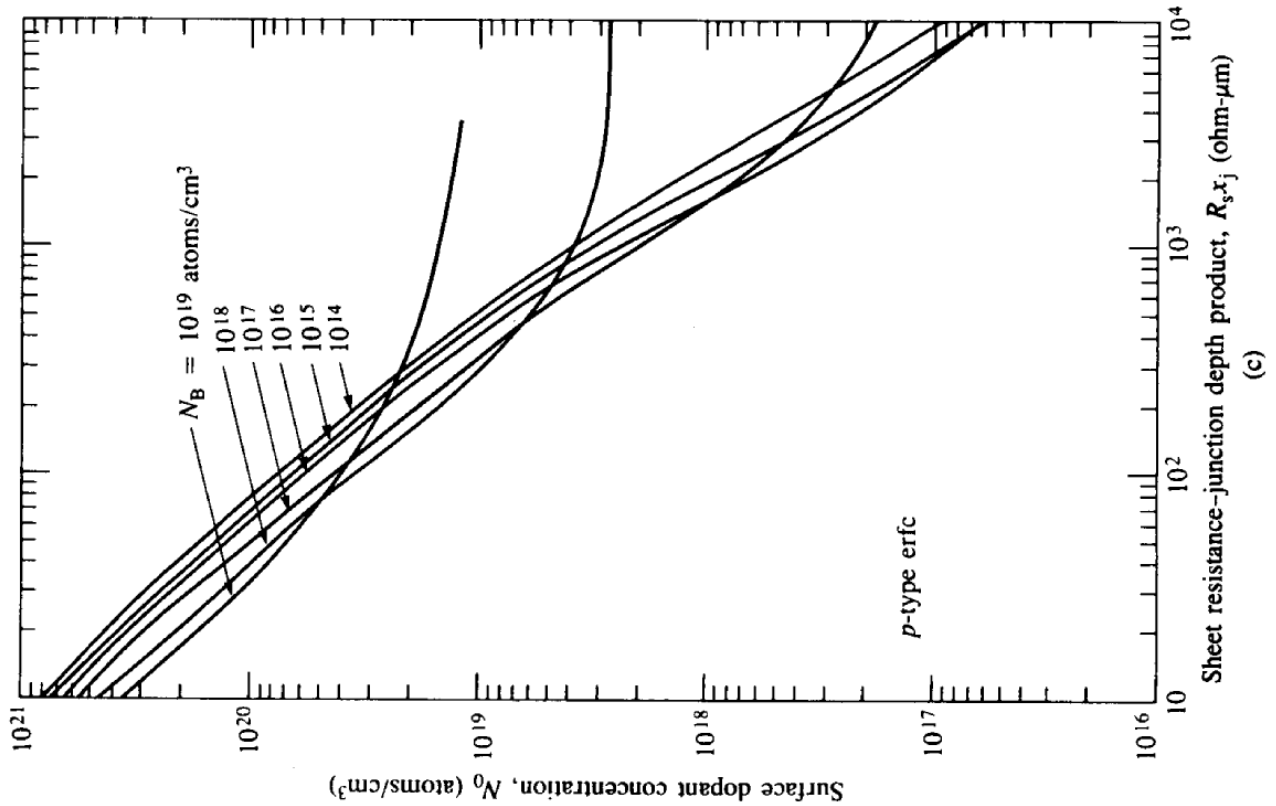
ELECTRONIC CROSS SECTIONS OF EISEN SCALED

ENERGY (KEV)	PROJECTED RANGE (MICRONS)	PROJECTED STANDARD DEVIATION (MICRONS)
10	0.0139	0.0069
20	0.0253	0.0119
30	0.0368	0.0166
40	0.0486	0.0212
50	0.0607	0.0256
60	0.0730	0.0298
70	0.0855	0.0340
80	0.0981	0.0380
90	0.1109	0.0418
100	0.1238	0.0456
110	0.1367	0.0492
120	0.1497	0.0528
130	0.1627	0.0562
140	0.1757	0.0595
150	0.1888	0.0628
160	0.2019	0.0659
170	0.2149	0.0689
180	0.2279	0.0719
190	0.2409	0.0747
200	0.2539	0.0775
220	0.2798	0.0829
240	0.3054	0.0880
260	0.3309	0.0928
280	0.3562	0.0974
300	0.3812	0.1017
320	0.4060	0.1059
340	0.4306	0.1098
360	0.4549	0.1136
380	0.4790	0.1172
400	0.5029	0.1206
420	0.5265	0.1239
440	0.5499	0.1271
460	0.5730	0.1301
480	0.5959	0.1330
500	0.6186	0.1358
550	0.6744	0.1424
600	0.7288	0.1484
650	0.7819	0.1539
700	0.8338	0.1590
750	0.8846	0.1636
800	0.9343	0.1680
850	0.9829	0.1721
900	1.0306	0.1758
950	1.0773	0.1794
1000	1.1231	0.1827

SILICON

PHOSPHORUS


$N_B = 10^{19}$ atoms/cm^3
10^{18}
10^{17}
10^{16}
10^{15}
10^{14}
p-type Gaussian
Surface dopant concentration, N_0 (atoms/cm^3)
10^{21}
10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
10
10^2
10^3
10^4
Sheet resistance – junction depth product, $R_s x_j$ (ohm-μm)
(d)


$N_B = 10^{19}$ atoms/cm^3
10^{18}
10^{17}
10^{16}
10^{15}
10^{14}
p-type erfc
Surface dopant concentration, N_0 (atoms/cm^3)
10^{21}
10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
10
10^2
10^3
10^4
Sheet resistance–junction depth product, $R_s x_j$ (ohm-μm)
(c)