EE143 Midterm Exam #2 Solutions **Fall 2003**

Problem 1

(a) (i)Let translational error be (x_t, y_t).

After subtracting the translational error, we have:

	Top	Right	Center	Left	Bottom
x		$+3 - x_t$	0	$-2 - x_t$	
y		$+3 - y_t$	0	$+1 - y_t$	

Since thermal run out/in error is antisymmetrical : $[+3 - x_t] = -[-2 - x_t]$ gives $\mathbf{x_t = +0.5\ \mu m}$

Since rotational error is antisymmetrical : $[+3 - y_t] = -[+1 - y_t]$ gives $\mathbf{y_t = +2\ \mu m}$

or

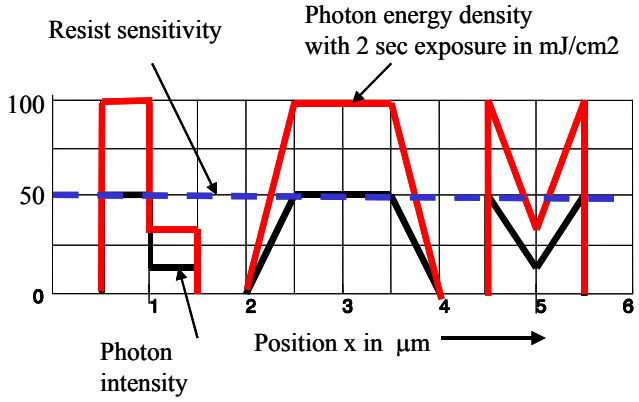
	Top	Right	Center	Left	Bottom
x		2.5	0	-2.5	
y		1	0	-1	

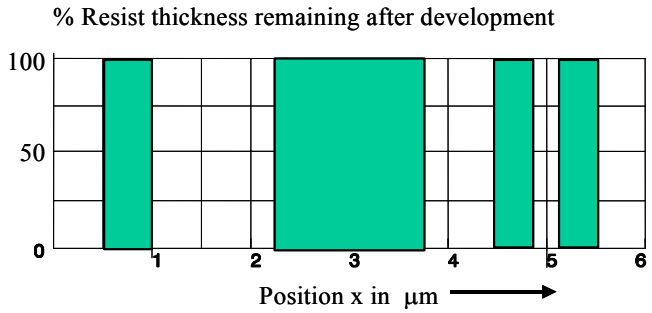
(ii) **thermal run out error = +2.5 μm**

(iii) **rotational error = +1 μm (counterclockwise)**

(b) DOF = $\frac{1}{2\lambda}(\frac{R}{k})^2$. Therefore DOF ratio **increases** by $(1/0.8)^2 - 1 = 0.56 =$ **56%**

(c) (i) **Negative resist** (ii) **Resist sensitivity = 50 mJ/cm^2**





Problem 2

(a)Geometrical shadowing is due to the original substrate topography. Self shadowing is due to the additional topography change with the deposited film.

(b) R = constant × exp $[-E_a/kT]$ or $E_a = -k \times \frac{\ln R(1) - \ln R(2)}{1/T(1) - 1/T(2)}$

R = 20000 Å/min at T =1073K

R = 2000 Å/min at T=973K

Therefore $\mathbf{E_a = 2.1eV}$

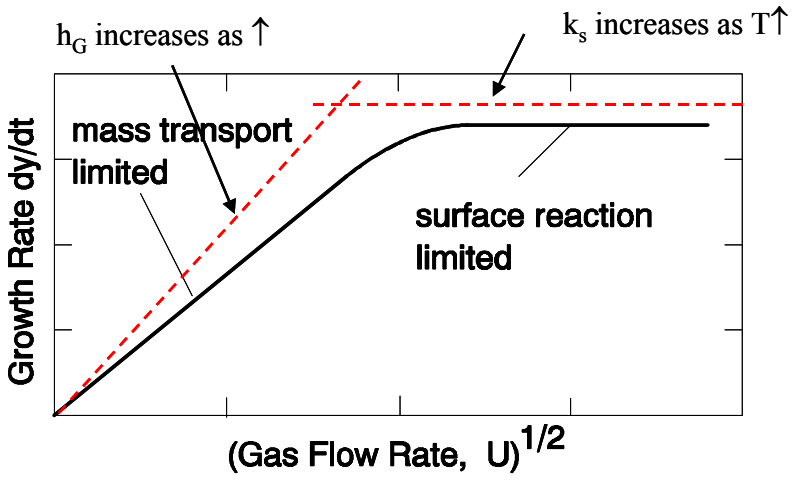
(c)(i) k_s is proportional to exp $[-E_a/kT]$. Higher T gives higher k_s.

(ii)

$h_G = \frac{D_G}{\overline{\delta}}$ with $D \propto T^{3/2}/P$ and $\overline{\delta} = \frac{2}{3}\frac{L}{\sqrt{\frac{\rho UL}{\mu}}}$

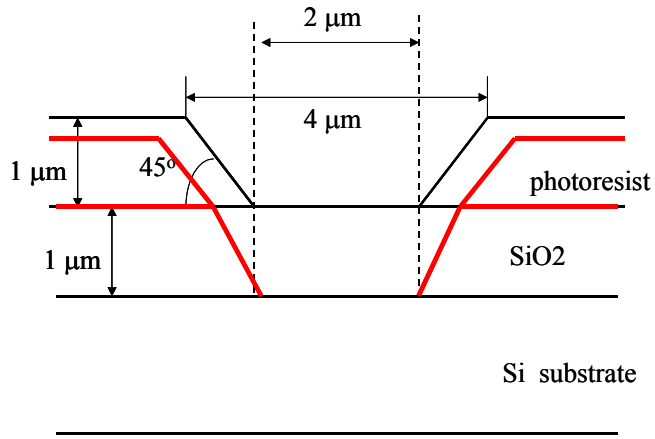
Since $\rho = P/kT$, therefore h_G increases with T when other control parameters are same.

(d) PECVD can be performed at a lower processing temperature than thermal CVD. The deposited film properties (mechanical stress, density, etc) can also be tailored with plasma and substrate bias conditions. Also possible to form special compound films which cannot be formed by thermally activated chemical reactions.



Problem 3

(a)(i)



(ii) Width of the opening at the top of the contact hole.= $2 + 2 \times(0.2+0.2 \cot 45^{o})$ = **2.8 μm** .

(iii) Width of the opening at the bottom of the contact hole = **2 μm** .

(b)

(i) **Minimum** etching time to clear all contact holes on a wafer.

$$= \text{nominal etching time} \times \frac{\text{max } SiO_2 \text{ thickness}}{\text{min oxide etching rate}} = \frac{1\ \mu m}{1\ \mu m/\text{min}} \times \frac{1.2}{0.9} = \mathbf{1.33\ min}$$

(ii) Si substrate will be exposed after etching the oxide for

$$\text{nominal etching time} \times \frac{\text{min } SiO_2 \text{ thickness}}{\text{max oxide etching rate}} = \frac{1\ \mu m}{1\ \mu m/\text{min}} \times \frac{0.8}{1.1} = 0.73\ \text{min}$$

Maximum depth of Si substrate etched.= 0.5 μm /min ×(1.33-0.73)min = **0.3 μm**

(c) By adding hydrogen to the CF_4 plasma , the F* radicals will be reduced due to the reaction : H+F*→ HF . Both etching rates for SiO_2 and Si will be reduced but Si etching rate is reduced more. During the oxide overetch time, the Si substrate etched is less than the pure CF_4 case.

Problem 4

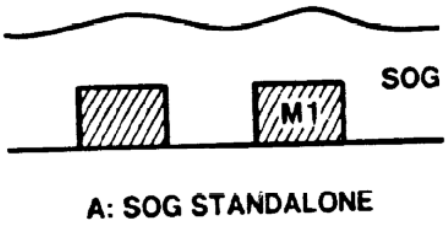
(a) RIE of aluminum lines is a series of three major process steps:

Step1 – removal of thin native aluminum oxide on surface using BCl_3 plasma

Step 2 – etching of aluminum film using chlorine based plasma

Step 3 – re-grow Al native oxide ***slowly*** using low oxygen content ambient [oxidation is exothermic].

(b) As a simple process flow, SOG is applied as a liquid on top of metal line patterns. Surface tension will give a relative flat SOG surface. The SOG is then cured at 400C to solidify, giving a solid dielectric.



A: SOG STANDALONE

Advantages- (A) Simple processing equipment, (B) SOG can be modified by adding different components.
Disadvantages – (A) Volume shrinkage during the curing step can generate large mechanical stress , (B) For thick SOG layers, outgassing during curing may trap bubbles.

(c):

	Deposition Method	Patterning Method
AlCu interconnect	Sputtering	RIE
W-plug	CVD	RIE or CMP
SiN etch stop	CVD	Wet etch or RIE
Cu interconnect	CVD or Plating	CMP
Cu plug	CVD or plating	CMP

(i) Typical Cu content of the Al-Cu alloy is 1-4at %. AlCu phase will precipitate in the grain boundaries during a sintering step which will block Al electromigration.
(ii) The W plug electrically connects two Al metal layers as a planarized contact via.
(iii) The SiOF dielectric has a lower dielectric constant than silicon oxides. This will reduce the RC time delay constant.
(iv) The SiN etch stop layers act as an etching mask and also as an etch stop for oxide RIE for the Dual Damascene process.