

Problem 1: Interconnect (10 points)

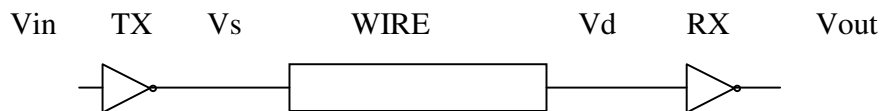
Consider the communication link shown below. The wire is 100mm long and has some characteristic resistance, capacitance, and inductance per unit length given by

$$r = 0.02 \text{ ohm/um}$$

$$c = 133 \text{ aF/um}$$

$$l = 333 \text{ fF/um}$$

The transmitter and receiver are both CMOS inverters with a 2.5V supply. However, the transmitter is designed by an inexperienced engineer using the same W/L ratio for the PMOS and NMOS transistors. As a result, the transmitter has an output impedance of 50 ohm when driving a high output, but only 20 ohm when driving a low output.



- a. What is the delay from a rising edge at V_{in} to V_{out} ? Assume that the inverters have negligible propagation delay (and capacitance), and that the RX inverter switches instantaneously when its input reaches $V_m = V_{dd} / 2$ (3 points)

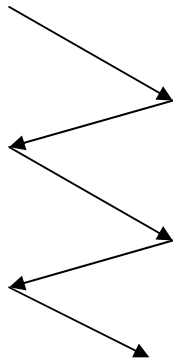
$t_p =$

- b. The link designer recognizes that the wiring resistance is slowing down the link. To improve the speed, the wire is redesigned with thicker, lower resistance metal until the resistance is negligible, but with the capacitance and inductance remaining unchanged. Complete the lattice diagrams below for a rising (0V to 2.5V) transition at V_{in} . Stop either at the end of the provided diagrams, or when V_s and V_d are both within 0.1V of their final values. Remember to note the times at which V_s and V_d change. **(4 points)**

$V_{in}: 0V \text{ to } 2.5V$

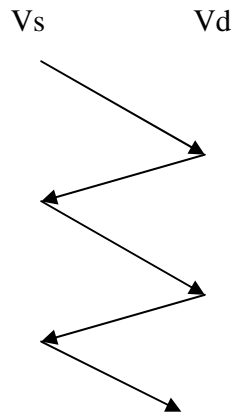
V_s

V_d



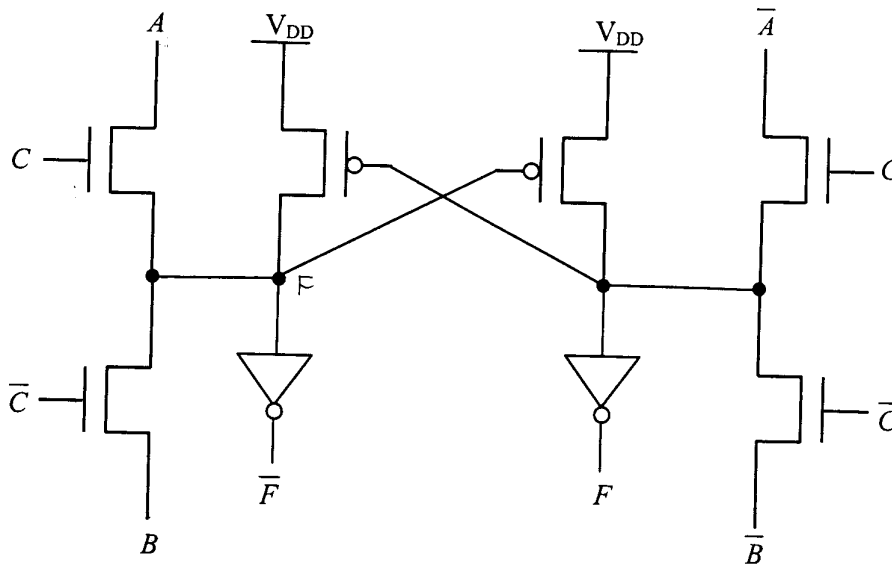
c. Do the same for a falling (2.5V to 0V) transition at V_{in} . (3 points)

$V_{in}: 2.5V \text{ to } 0V$



Problem 2: Complementary Pass-Transistor Logic (9 points)

Consider the complementary pass-transistor logic shown below. It accepts three inputs A, B, C and their complements, produces the output F and its complement.



a. Fill out the following truth table (2 points)

A	B	C	F
0	0	0	
1	0	0	
0	1	0	
1	1	0	
0	0	1	
1	0	1	
0	1	1	
1	1	1	

b. Write down the Boolean function this circuit implements in the given space below. Make sure to simplify the logic expression to its minimal form. Explain in one sentence the function of this circuit. (2 points)

F =

c. Explain the purpose of the two PMOS transistor in the circuit. **(1 point)**

d. Now we want to implement the same function using **dynamic logic** with a **PMOS pull up network**. Draw the implementation schematic. You may assume the inputs are available in inverted and non-inverted format. However, you are only required to produce F at the output (in other words, the gate does NOT have to be complementary). **(2 points)**

e. Determine the logical effort of the gate you just designed. **(2 points)**

Hint: size the gate first such that a current drive identical to a minimum sized CMOS inverter is obtained.

Problem 3: Arithmetic (11 points)

Designer Viterbi, working for a famous telecommunications company has to implement a digital hardware module that implements the following logic function:

$f = (a > b) ? a : b$. In other words, the output f should be equal to a if $(a > b)$, else it should equal b . Both a and b are N -bit 2's complement numbers.

- a. Draw a block diagram of how you think this function should be implemented. Do not show any transistors. Use only gates and higher level modules, such as for instance $M \times N$ multipliers. **(4 points)**

- b. Highlight or draw (using arrows) **the longest delay path** on your block diagram. Determine one of the possible set of input values that would trigger that longest path. (3 points)

- c. Derive an expression for the **worst-case delay of the module as a function of N and the delay of the composing gates or modules** (such as t_{carry} of full adder, t_{NAND}). Make sure to clearly define each parameter you use in your expression. (2 points)
- d. Propose one possible way on how you would speed up that design (the faster the better). Redraw your block diagram. (2 points)