

**EECS 141: Fall 1992 - MIDTERM 2****J.M. Rabaey**

For all the problems, you can assume the following transistor parameters:

NMOS:

$$V_{Tn} = 0.75V, K_n = 20 \mu A/V^2, \text{LAMBDA} = 0.05, \text{GAMMA} = 0.5 V^{1/2}, 2\text{PHI}_F = -0.6V$$

PMOS:

$$V_{Tp} = -0.75V, K_p = 7 \mu A/V^2, \text{LAMBDA} = 0.1, \text{GAMMA} = 0.5 V^{1/2}, 2\text{PHI}_F = -0.6V$$

NPN:

$$\beta_F = 100, V_{BE(on)} = 0.7V, V_{BE(sat)} = 0.8V, V_{CE(sat)} = 0.1V, I_S = 10^{-17}A$$

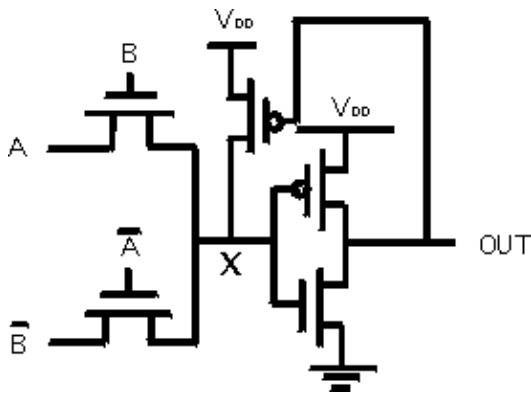
For all problems, you may assume that the MOS transistor lengths indicated are the effective lengths ( $L_{eff}$ ) or, equivalently, that  $LD = 0$ .

**Problem 1: Logic Gates**

The circuits shown below have a major problem. For each of those circuits,

- Determine its logic function.
- Explain the problem.
- Redraw the circuit such that the problem is solved. Try to keep the number of changes minimal (e.g. if a circuit is dynamic, keep it such). Also, stick to the available input signals.

Circuit 1:



a). Logic function:

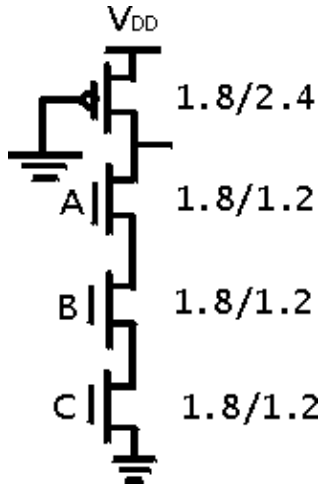
A	B	X	OUT
0	0	1	0
0	1	0	1
1	0	?	?
1	1	1	0



-->  $W/L_p \ll W/L_n$  so say  $W/L_p = 1.8/2.4$   
 Ideally, we'll set the ratio to make  $V_{OL} < V_{Tn}$

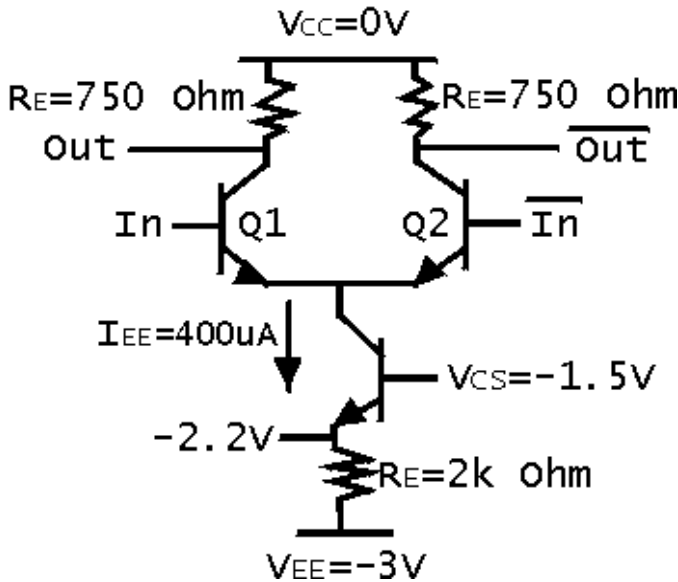
Note: It is true that  $t_{PHL}$  and  $t_{PLH}$  are asymmetric, but this is almost always true for pseudo NMOS. It is not correct to set  $R_{PMOS} = R_{NMOSCHAIN}$  because then  $V_{OL} = V_{DD}/2$ .

c). Redrawn Circuit:



### Problem 2: Differential Current Mirror Logic

A differential CML gate is shown below.



a). Determine the important points of the VTC ( $V_{OH}$ ,  $V_{OL}$ ,  $V_{IH}$ ,  $V_{IL}$  and  $V_M$ ). For the computation of  $V_{IH}$  and  $V_{IL}$ , you can use the simplified definition ( $V_{IL}$  is defined as the point where the transistor Q1 is carrying 1% of the current through the current source, while at  $V_{IH}$  transistor Q1 carries 99% of the total current).

$V_{OH}$ ,  $V_{OL}$ : Assume the current in Q1 and Q2 is  $I_{EE}$  or zero.  
 Current = 0 -->  $V_{OH} = V_{CC} = 0$   
 Current =  $I_{EE}$  -->  $V_{OL} = V_{CC} - I_{EE}R_C = -0.30V$

$V_M$ : This is a symmetric differential circuit, so  $V_M = (V_{OL} + V_{OH}) / 2 = -0.1V$

$V_{IH}, V_{IL}$ : Remember, this is a differential circuit, so  $I_n$  and  $I_p$  changes.

When  $V_{In} - V_{Ip} = 120mV$ ,  $I_{C1} = 100 I_{C2}$

So,  $V_{IH} = V_M + 60mV = -0.09V$

$V_{IL} = V_M - 60mV = -0.21V$

b). Assume that the output **Out** connects the input terminal of 5 identical gates (or has a fanout of 5). Recompute the values of  $V_{OH}$  and  $V_{OL}$  under these conditions.

When an output is low base current inot load = 0.

So  $V_{OL}$  stays at  $-0.30V$ .

When output is high, each load draws base current =  $400\mu A / B_F = 4mA$

So,  $V_{OH} = 0 - 5 \times 4mA \times 750\Omega = -0.015V$

c). Assume that the capacitance to the outputs of the gate equals  $40fF$  and that there are no other capacitors in the circuit. You can ignore  $Q_F$ . Compute the power consumption of the gate. Assume that the input is high 50% of the time and makes a transition (L  $\rightarrow$  H or H  $\rightarrow$  L) every 5 nsec. Assume that the input is high for 50% of the time.

$P_{static} = I_{EE} (V_{CC} - V_{EE}) = (400\mu A)(3V) = 1.2mW$

$P_{dynamic}$ : with each transition, one  $40fF$  capacitor is charged.

Energy/Transition =  $(V_{CC} - V_{EE})(V_{OH} - V_{OL}) C_L = (3V)(0.3V)(40fF) = 36fJ$

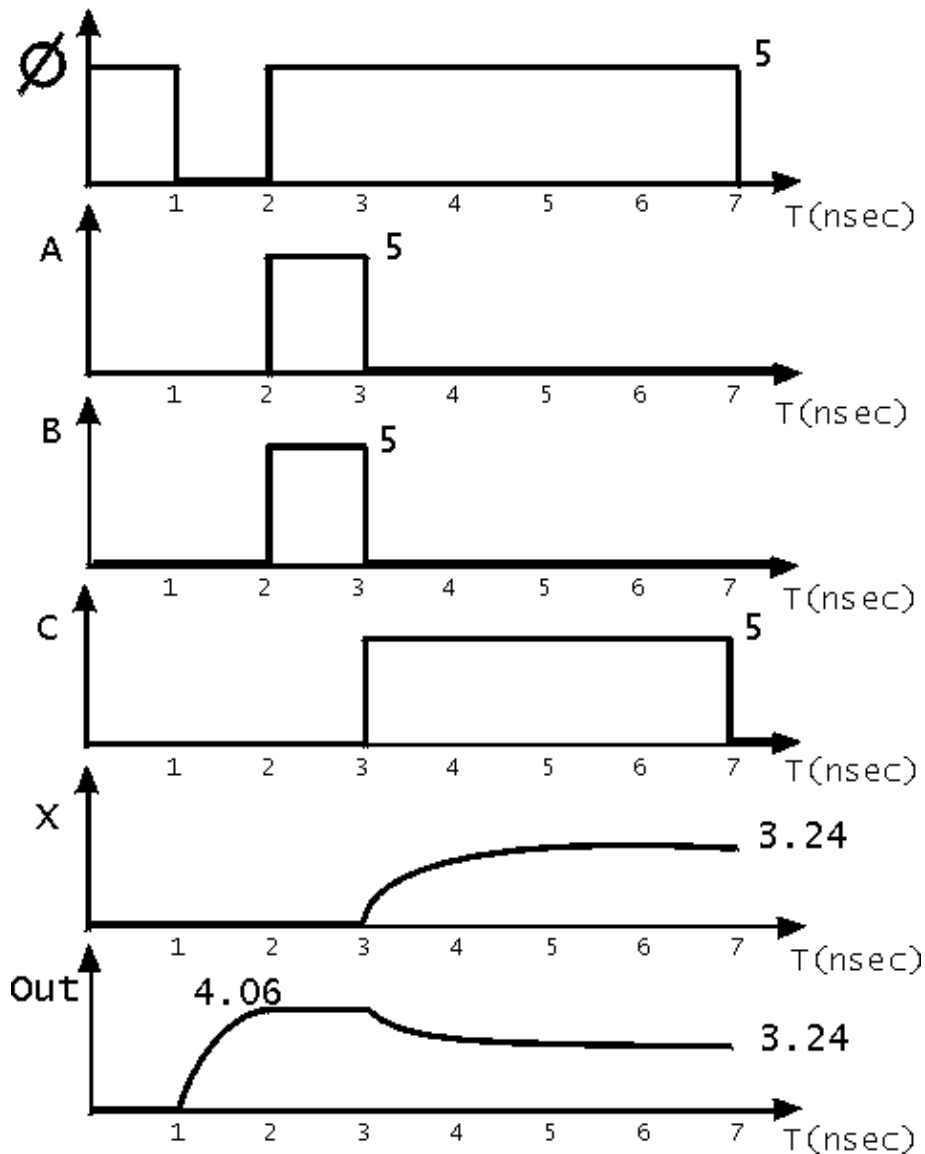
Hence,  $P_{dynamic} = 36fJ/5nsec = 7.2\mu W$

$P_{total} = P_{static} + P_{dynamic} \sim P_{static} = 1.2mW$

### Problem 3: Dynamic CMOS

After taking EE141, a student figured out that dynamic circuits were way too complex and came up with his "new" dynamic style called BDL (for Berkeley Dynamic Logic). A gate in this logic style is shown in the Figure below.





$t = 1\text{ ns} \rightarrow 2\text{ ns}$ :  $40\text{fF}$  charging through PMOS at **Out**; no charge at **X** (floating)

$$V_{\text{out}} = 5(1 - \exp(-(t-1\text{ns})/(15\text{k}\Omega \times 40\text{fF})))$$

$$V_{\text{out}}(2\text{ns}) = 5(1 - \exp(-1\text{ns}/0.6\text{ns})) = 4.06$$

$t = 2\text{ ns} \rightarrow 3\text{ ns}$ : Output floating  $\rightarrow$  no change in voltage

**X** tied to ground  $\rightarrow$  no change in voltage.

$t = 3\text{ ns} \rightarrow 7\text{ ns}$ : Charge is shared from **Out** to **X**.

$$\text{Equilibrium voltage} = (40/40+10)(4.06) = 3.24\text{V}$$

After 4ns, should be very close to equilibrium.

c). TRIVIA: Are the Following Statements TRUE or FALSE?

T	F
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x		Clock Feedthrough Can be Reduced by Reducing the Size of precharge Transistor.
	x	NAND logic is preferred over NOR logic in dynamic Gates with NMOS PDN.
x		Implementing a NAND function is Not possible in DOMINO.
	x	Dynamic Logic is the Logic Style with the Smallest Number of Transistors
	x	The Propagation Delay of a Dynamic Gate is Linear with Respect to Fanin.
x		Clock FeedThrough Can Hurt the Power Consumption.
		Increasing the Fanout of a Dynamic Gate Does Not Affect the Noise Margins.
	x	Dynamic Logic is Often Used in Portable Cameras for Its Low Power Consumption.

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