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6:30-8:00pm

EECS 141: FALL 2007—MIDTERM 2

For all problems, you can assume the following transistor parameters (unless mentioned otherwise):

NMOS:
$V_{Tn} = 0.4$, $k'_n = 115\ \mu A/V^2$, $V_{DSAT} = 0.6V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2\Phi_F = -0.6V$
PMOS:
$V_{Tp} = -0.4V$, $k'_p = 30\ \mu A/V^2$, $V_{DSAT} = -1V$, $\lambda = 0$, $\gamma = -0.4\ V^{1/2}$, $2\Phi_F = 0.6V$

NAME	Last Solutions First

GRAD/UNDERGRAD	

Problem 1: _____/20

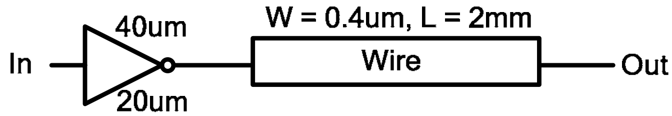
Problem 2: _____/22

Problem 3: _____/17

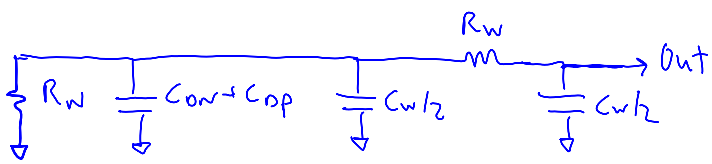
Total: _____/59

PROBLEM 1. Wires and Elmore Delay (20 points)

For this problem, you should assume that all of the transistors are minimum channel length (L=0.25µm) and have the following characteristics: C_G = 2fF/µm, C_D = 1fF/µm, and $R_{sqn} = R_{sqp}/2$ = 15kΩ/□. For the wires, you should assume that C_{wpp} = 0.1fF/µm^2, $C_{wfringe}$ = 0.05fF/µm/edge, and R_w = 0.1Ω/□



a) **(5 pts)** Draw the RC model you would use to calculate the delay of the circuit shown above from In rising to Out falling. You should replace the wire with a single section Π model and calculate the values of the R's and C's in your model.



$R_N = 15k\Omega \cdot \frac{0.25\mu m}{20\mu m} = 187.5\ \Omega$

$C_w = 0.4\mu m \cdot 2000\mu m \cdot 0.1fF/\mu m^2 + 2 \cdot 2000\mu m \cdot 0.05fF/\mu m$

$C_{DN} + C_{DP} = 60\mu m \cdot 1fF/\mu m = 60fF$

$C_w = 280fF$

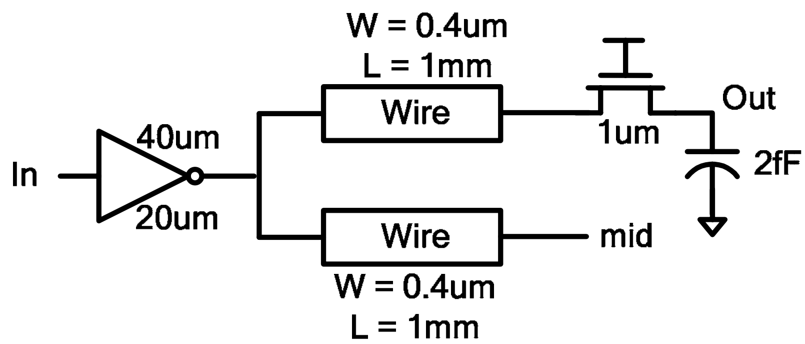
$R_w = 0.1\Omega \cdot \frac{2000\mu m}{0.4\mu m} = 500\Omega$

b) **(3 pts)** Using this model and assuming a ramp input (i.e., $t_p = \tau_{Elmore}$), what is the delay from In rising to Out falling?

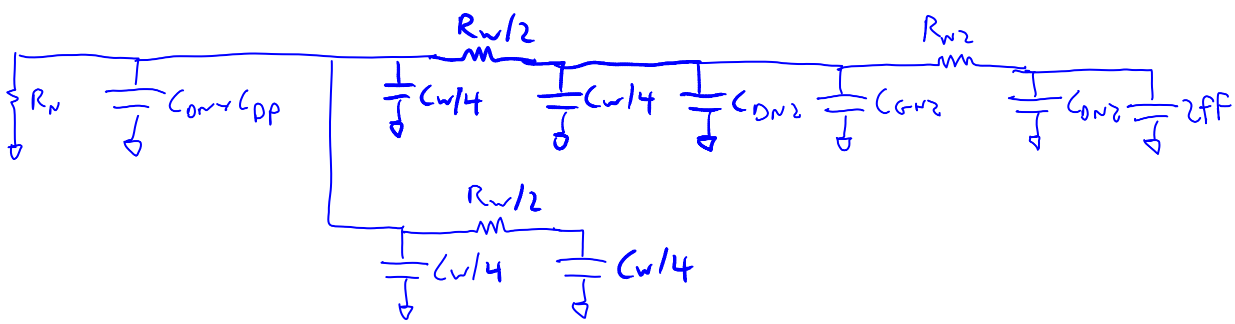
$\tau_{elmore} = R_N \cdot \left(C_{DN} + C_{DP} + \frac{C_w}{2}\right) + (R_N + R_w) \cdot \frac{C_w}{2}$

$\tau_{elmore} = 187.5\Omega \cdot (60fF + 140fF) + 687.5\Omega \cdot 140fF$

$\rightarrow t_p = 133.75ps$



c) **(12 pts)** What is the ramp delay from In rising to Out falling for the circuit shown above? You do not need to provide a numerical answer for this problem – you only need to provide the equation you would use to calculate the delay, and the values of the R's and C's in that equation. You can assume that Out is initially charged to V_{DD}, and you can model each of the wires with a single section Π model.



$R_N = 187.5\,\Omega$

$C_{ON}+C_{OP} = 60fF$

$C_W = 280\,fF$

$C_{ON2} = 1\mu m \cdot 1fF/\mu m = 1fF$

$C_{GN2} = 1\mu m \cdot 2fF/\mu m = 2fF$

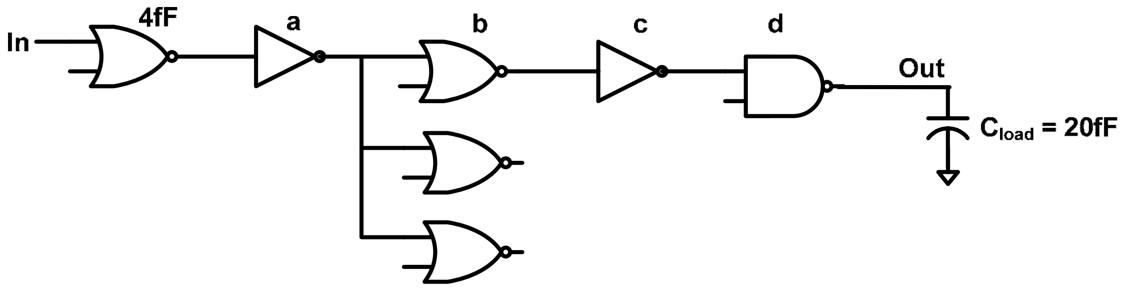
$R_{N2} = 15k\Omega \cdot \frac{0.25\mu m}{1\mu m} = 3.75k\Omega$

$R_W = 500\,\Omega$

$$\tau_{elmore} = R_N\left(C_{ON}+C_{OP}+\frac{C_w}{4}+\frac{C_w}{4}\right) + R_N\frac{C_w}{4} + \left(R_N+\frac{R_w}{2}\right)\cdot\left(\frac{C_w}{4}+C_{ON2}+C_{GN2}\right)$$
$$+\left(R_N+\frac{R_w}{2}+R_{N2}\right)\cdot\left(C_{ON2}+2fF\right)$$

$t_p = \tau_{elmore}$

PROBLEM 2. Logical Effort and Gate Sizing (22 points)



a) **(6 pts)** What is the path effort from In to Out?

$F = \frac{20fF}{4fF} = 5$

$\Pi LE = \frac{5}{3} \cdot \frac{5}{3} \cdot \frac{4}{3} = \frac{100}{27}$

$\Pi B = 3$

$PE = F \cdot \Pi LE \cdot \Pi B = \frac{500}{9}$

$PE = 55.556$

b) **(2 pts)** What EF/stage minimizes the delay of this chain of gates?

$EF/stage = PE^{1/5}$

$EF/stage = 2.233$

c) **(8 pts)** Size the gates to minimize the delay from In to Out.

$\frac{4}{3} \cdot \frac{20fF}{d} = 2.233 \longrightarrow d = 11.94$

$\frac{d}{c} = 2.233 \longrightarrow c = 5.35$

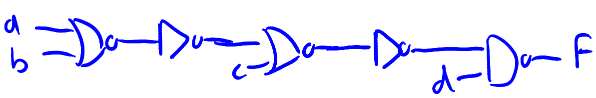
$\frac{5}{3} \cdot \frac{c}{b} = 2.233 \longrightarrow b = 3.99$

$3 \cdot \frac{b}{a} = 2.233 \longrightarrow a = 5.36$

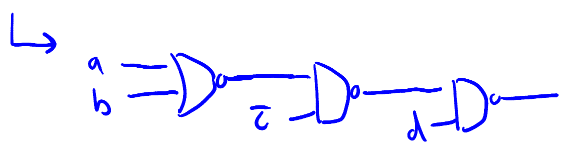
Size	Value (fF)
a	5.36
b	3.99
c	5.35
d	11.94

d) **(6 pts)** Both the delay and the power consumption of this gate chain of gates can be reduced by changing the number of stages and/or the types of gates used in the chain (but still implementing the same logic function). Please draw an improved (from both a power and delay standpoint) schematic for this chain of gates. You do not need to provide transistor sizes. (Hint: What would be the optimal number of stages for a chain of gates with the path effort you calculated?)

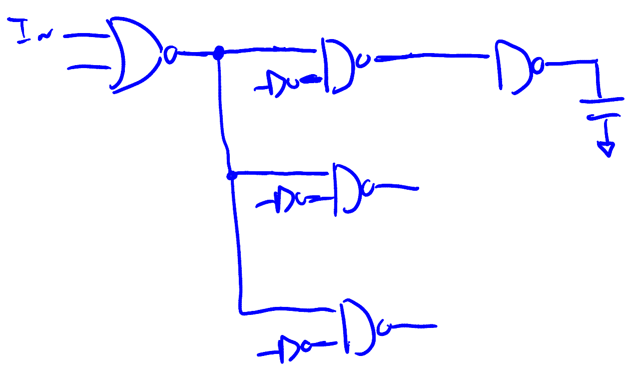
Optimal # of stages is $\log_4(PE) \approx 2.9$. So, need to reduce the number of stages to 3, but maintain logical equivalence:



$$F = \overline{(a+b+c)\cdot d}$$

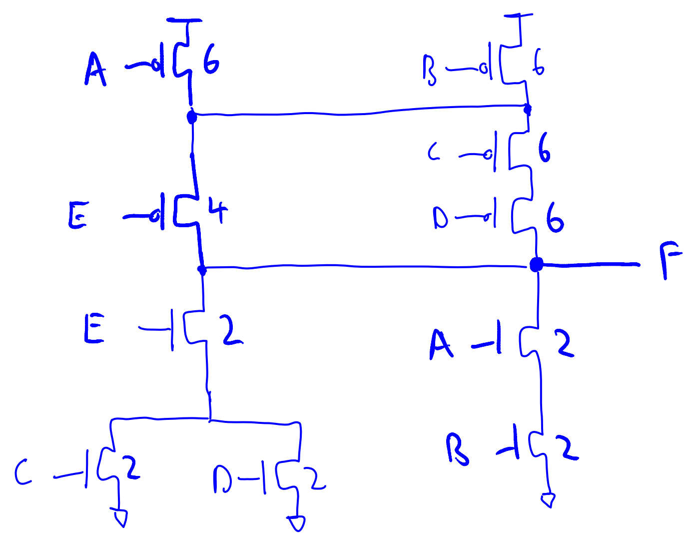


So, the complete improved chain would be:

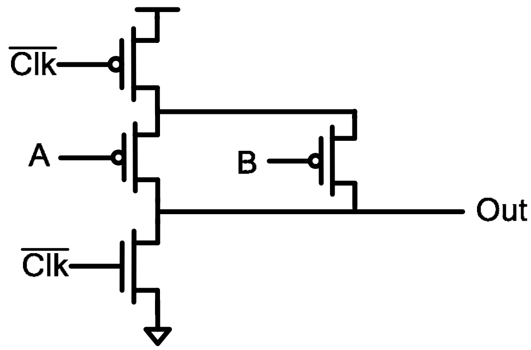


PROBLEM 3. Logic Styles (17 points)

a) **(6 pts)** Implement the function $F = \overline{(A \cdot B) + (C+D) \cdot E}$ with a complex static CMOS gate. You should arrange your gate to minimize the delay from the E input, and so that the worst-case pull up resistance is equal to the worst-case pull-down resistance.

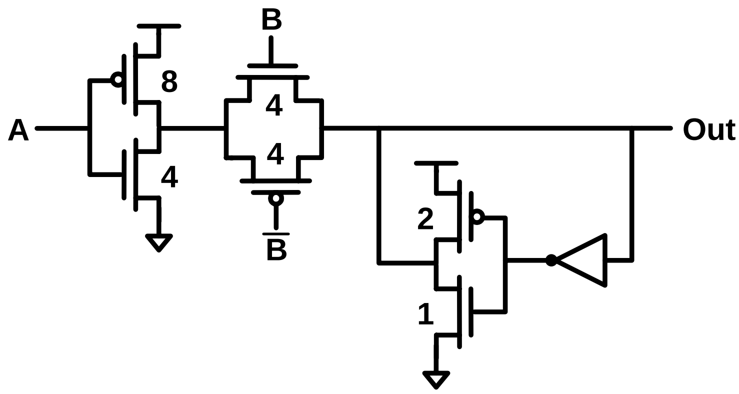


b) **(3 pts)** What is the logic function performed by the dynamic gate shown below?



$Out = \bar{A} + \bar{B}$

$\boxed{\text{NAND gate}}$



c) **(8 pts)** What is the LE of the gate shown above from the B input?

Just like keepers, feedback inverter takes current away from charging the output. So:

$$R_{drive} = \frac{1}{4}R_{sqN} + \frac{1}{4}R_{sqN} = \frac{1}{2}R_{sqN}$$

$$R_{keeper} = R_{sqN}$$

$$R_{gate} = \frac{1}{\frac{1}{R_{drive}} - \frac{1}{R_{keeper}}} = R_{sqN}$$

$$C_{gate} = 4C_g$$

$$R_{inv} = R_{sqN} \qquad C_{inv} = 3C_g$$

$$LE_B = \frac{4R_{sqN}C_g}{3R_{sqN}C_g} \qquad \boxed{LE = \frac{4}{3}}$$