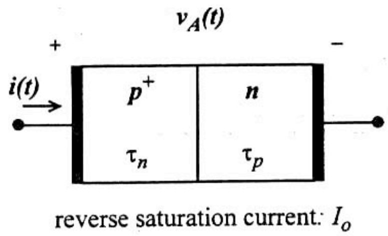
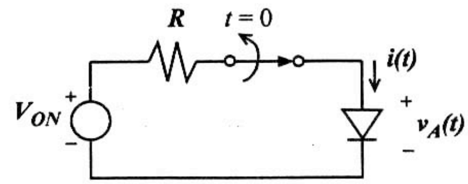
Problem 1 [20 points]

Consider an ideal p^+-n step junction diode in the following circuits:

IDEAL DIODE



DIODE CIRCUIT



The switch is closed for all times $t < 0$, then opened at time $t = 0$.
Assume that $V_{ON} >> v_A$ so that $i(t) = V_{ON} / R$ for times $t < 0$.

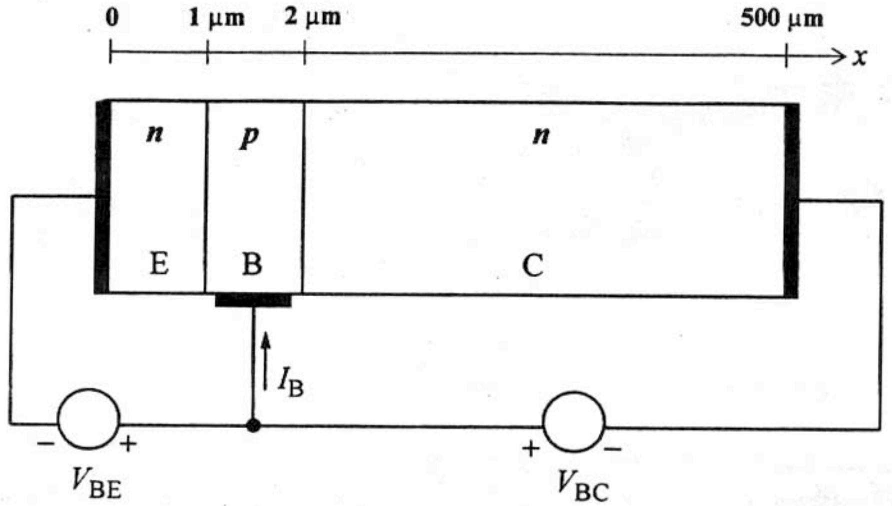
a) What is the stored hole charge, Qp, inside the diode, for times $t < 0$?

b) Derive an expression for Qp(t), for times $t > 0$

c) Derive an expression for $v_A(t)$, for times $t > 0$.

(Assume that the stored charge decays quasi-statically, i.e. the relationship between Qp and v_A is the same as in steady state.)

Problem 2 [40 points]
Consider the following npn bipolar transistor:



Assume that each region is uniformly doped, and that both the emitter and base are short, while the collector is long.

Doping concentrations: $N_E = 10^{19}cm^{-3}$, $N_B = 10^{17}cm^{-3}$, $N_C = 10^{15}cm^{-3}$
Minority carrier diffusion constants: $D_E = 2cm^2/s$, $D_B = 19cm^2/s$, $D_C = 12\ cm^2/s$
Minority carrier lifetimes: $\tau_E = \tau_B = \tau_C = 10^{-6}cm^2$.

The area of the transistor $A = 10^{-6}cm^2$.

a) Will this BJT suffer severe base-width modulation under forward active bias operation?

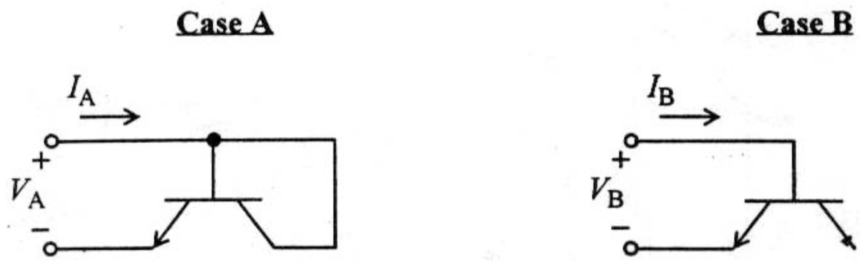
For the remaining sections of this question, consider the case where $V_{BE}=V_{BC}=0.6V$

b) Sketch the energy band diagram. (Indicate the Fermi levels in the quasi-neutral regions.)

c) Sketch the excess minority carrier densities in each region: $p'_E(x)$, $n'_B(x)$, and $p'_C(x)$. Write the expressions for those. (You may ignore the widths of the depletion regions.)

d) What is the value of the base current, I_B, assuming no recombination in the base?

Problem 3 [25 points]
Consider the following two ways to connect an npn BJT as a diode:



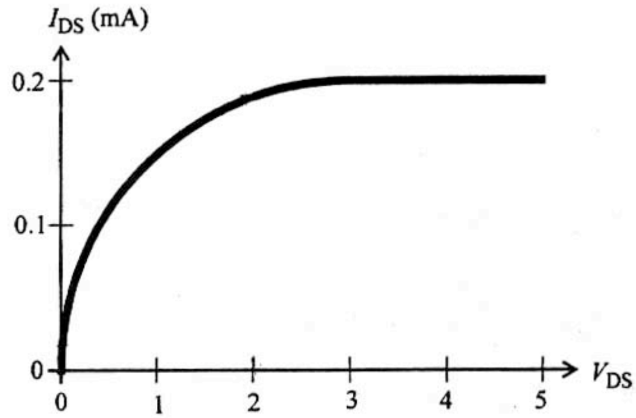
a) Derive the I-V relationship for each "diode" from the Ebers-Moll equations. I_A or I_B should be expressed only in terms of V_A or V_B and the Ebers-Moll parameters (α_F, α_R, I_{ES}, I_{CS}).

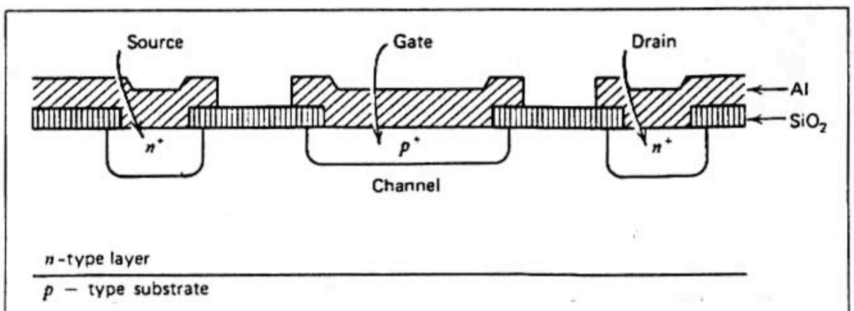
b) Assume the $V_A >> kT/q$ and $V_B >> kT/q$. Sketch the excess minority carrier concentration in the base for each case, indicating the values of n'_B at the edges of the depletion regions.
(Assume that the base region of each transistor is short.)
Note: For case B, you should use the Ebers-Moll equations to find $[\exp(qV_{BC}/kT)-1]$ in terms of $V_B=V_{BE}$.

c) Which connection seems most appropriate for use as a diode? Why?
(Hints: Compare the switching times for the two cases.)

Problem 4 [15 points]

The following plot is the room-temperature I-V characteristic of an ideal planar Si n-channel JFET with W = 10 μm and L = 5 μm and channel doping concentration $N_d = 10^{16} cm^{-3}$.





Schematic Cross-Sectional View of JFET

a) Estimate the turn-off voltage, V_T, from the plot above.

If you did not obtain an answer for part (a), use V_T = -2V for the remainder of this question.

b) What is the thickness of the channel, t? Assume that the gate region is degenerately doped p-type, and that the width of the depleting region at the channel-substrate junction can be neglected.

c) Sketch the I-V curve corresponding to V_{GS} = -1V on the plot provided. (Indicate values for V_{DS} at the pinch-off point, and I_{DSAT})
You may use the empirical model:

Sketch the I-V curve on the plot below. [6 pts]