Name:	**Student ID #:**

University of California at Berkeley
Electrical Engineering and Computer Science
EE105 Midterm Examination #2
April 16, 2014
(50 minutes)

CLOSED BOOK; Two standard 8.5" x 11" sheet of notes (both sides) permitted

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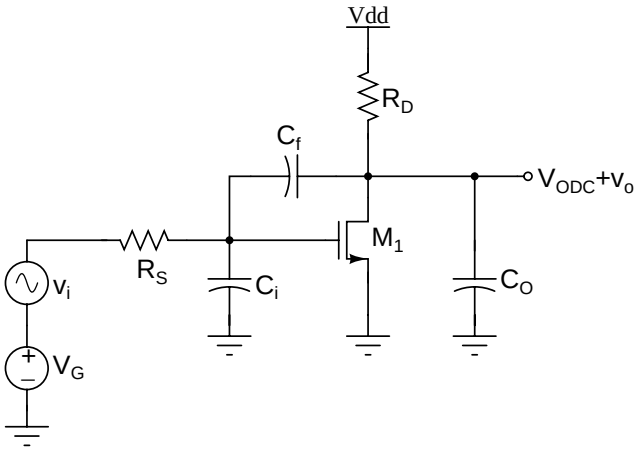
IMPORTANT NOTES

- Read each problem completely and thoroughly before beginning to work on it
- Summarize all your answers in the boxes provided on these exam sheets
- Show your work in the space provided so we can check your work and scan for partial credit
- Remember to put your name in the space above

Problem #	Points Possible	Score
1	60	
2	40	
Total	100	

1. (60 points) Frequency Response. For the circuit shown below, assume M_1 operates in saturation and has the following defining parameters: W, L, μ_n, C_{OX} , V_{TH} and λ.



(a) (8 points) Express the small-signal parameters g_m and r_o for M_1 for the DC bias condition V_G>V_{TH} in terms of the defining parameters and V_G.

(b) (8 points) Draw the small signal model for the circuit shown above.

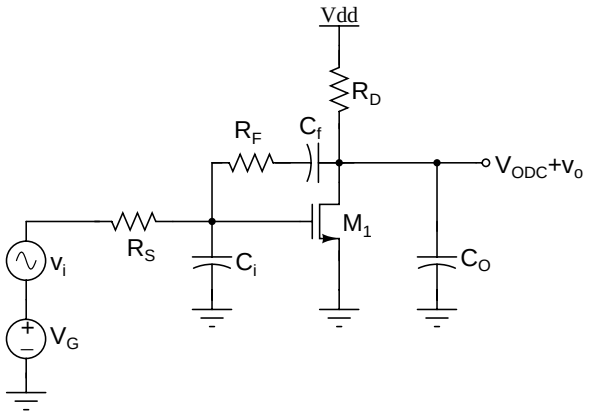
(c) (16 points) Determine the small signal transfer function $H(j\omega) = \frac{v_o(j\omega)}{v_i(j\omega)}$. Use only the capacitors explicitly shown. Assume $r_o > R_L$ for simplicity.

(d) (8 points) From the transfer function, identify the location of poles and zeros assuming that $g_m R_L \gg 1$.

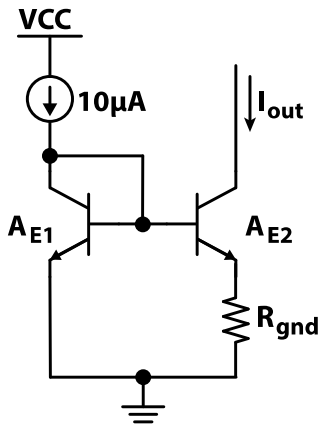
(e) (8 points) We know that at low frequencies, the output is 180° out of phase with respect to input. As the input frequency increases, there is additional phase added due to the pole(s) and zero(s). Now, what is the phase of $H(j\omega) = v_o/v_i$ at very high frequencies ? *(hint: The zero also does something interesting)*

(f) (6 points) You will learn in later courses (if you still want to stay in EE ☺) that this kind of a zero is actually a bad thing. One way to get rid of it is with the circuit shown below. From the transfer function you obtained above, find only the new location of zero including R_F *(hint: Just modify* $\frac{1}{j\omega C_F}$ *to* $\frac{1}{j\omega C_F} + R_F$*)*

(g) (6 points) Find the value of R_F that will cancel the bad zero completely.

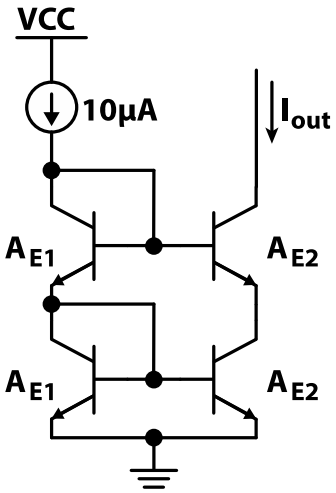


2. (30 points). DC bias calculations. For the circuit shown below, assume R_{gnd}=0, V_A=∞ and β is large enough to neglect the base current.



(a) (6 points) Find the relation between A_{E1} and A_{E2}, so that I_{out} =1mA.

(b) (10 points) With your sizing in Part (a), you discover that the current I_{out} is only 90% of 1mA. After a lot of debugging, you discover that the ground connection of the mirror transistor is improper and has a resistance R_{gnd} as shown. Find the value of R_{gnd}.



(c) (14 points) In order to boost the output impedance, we now utilize a cascode current source. With your sizing in (a) for A_{E2}, $V_A=\infty$ and $\beta=100$, find the value of I_{out}. Note that β is finite. (Hint: Express the emitter, base and collector currents of each transistor in terms of I_{out}).