# EE 105 Final Exam

Spring 2007                          Prof. Ming C. Wu                          May 11, 2007
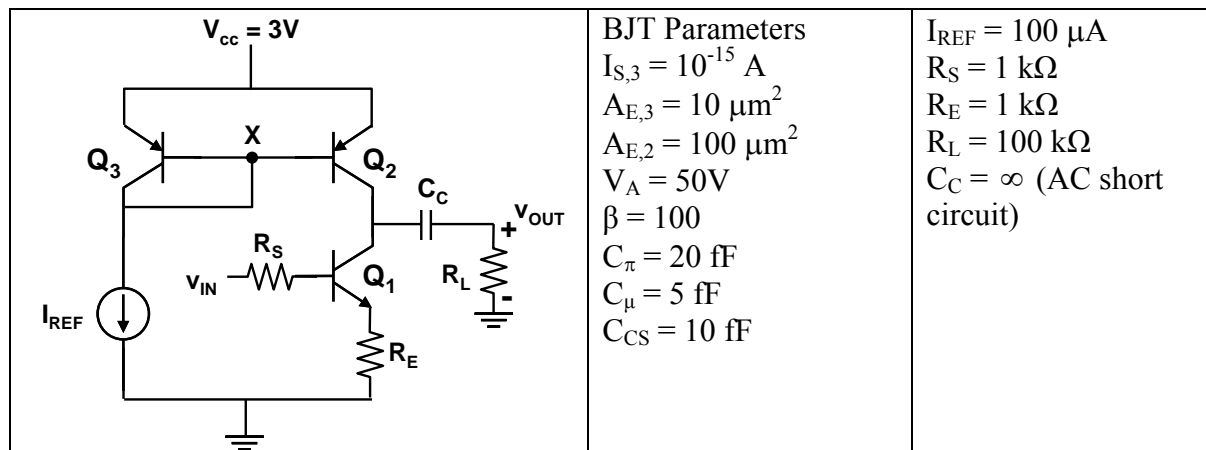
**Guidelines**

- Open book, open notes.
- You may use a calculator.
- No cell phone or other electronic devices are allowed.
- Show all your work and reasoning on the exam in order to receive full or partial credit.
- The problem may contain more information than you need. Just use the conditions that you think is necessary for the solution.
- Exam Time: 180 minutes

**(1)** Please answer the following questions.
   a) [2 pt] (Single choice) The drain current in a PMOS FET is conducted by (A) electron, (B) hole, (C) both.
   b) [2 pt] (Single choice) The drain current in a NMOS FET is conducted by (A) electron, (B) hole, (C) both.
   c) [3 pt] (Single choice) The collector current in an NPN bipolar transistor is conducted by (A) electron, (B) hole, (C) both.
   d) [3 pt] (Single choice) The collector current in a PNP bipolar transistor is conducted by (A) electron, (B) hole, (C) both.
   e) [5 pt] What is the flatband voltage of an MOS capacitor with a p-type substrate (doping = $10^{15}$ cm$^{-3}$), a heavily doped p-type polysilicon gate, and a high-k dielectric with a thickness of 10 nm and a dielectric constant of 30.
   f) [5 pt] For an NMOS with a substrate doping of $10^{15}$ cm$^{-3}$ (you have to determine the doping type yourself), a heavily doped n-type polysilicon gate, a 10-nm-thick oxide (dielectric constant = 3.9), find the *voltage drop across the oxide* when the NMOS is biased at the onset of inversion (i.e., at threshold).
   g) [5 pt] The small-signal equivalent circuit of a forward-biased P-N junction diode is a resistor. What is the resistance value when the diode is biased at 10 mA? Assume both N and P doping concentrations are $10^{16}$ cm$^{-3}$. The area of the diode is 100μm x 100μm.
   h) [5 pt] The small-signal equivalent circuit of a reverse-biased P-N junction diode is a variable capacitor. What is the capacitance tuning ratio (i.e., the ratio of the maximum and the minimum capacitance) if the bias is varied from -1V to -10V? Assume both N and P doping concentrations are $10^{16}$ cm$^{-3}$. The area of the diode is 100μm x 100μm.
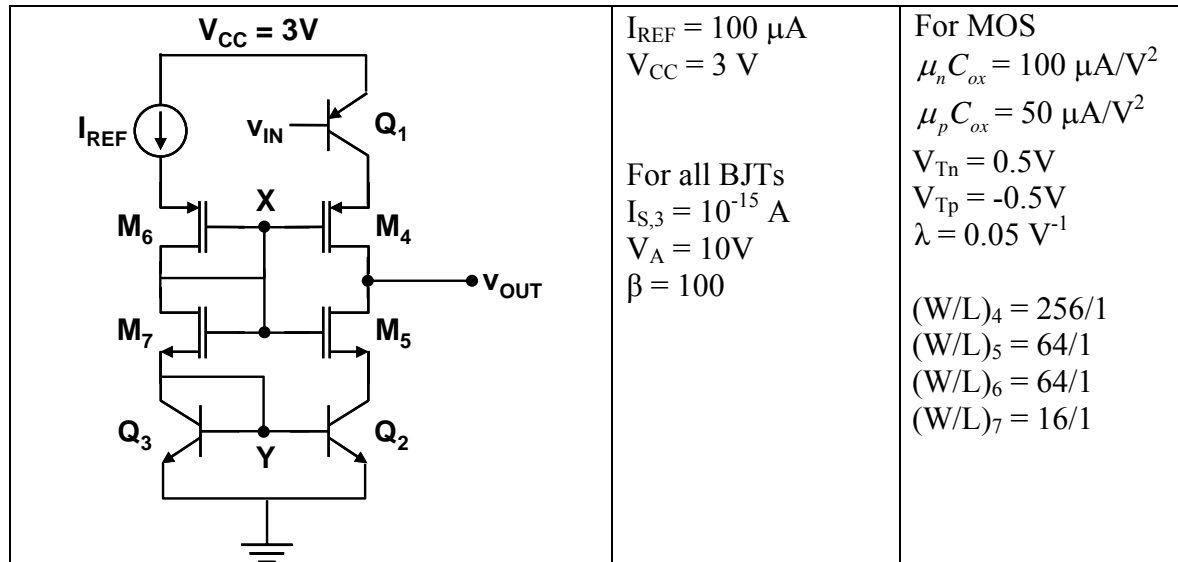
**(2)** For the bipolar amplifier shown in the following. Ignore base current for Part a) to d).
   a) [5 pt] What is the DC voltage at node X?
   b) [5 pt] Calculate the small-signal parameters (i.e., $g_m$, $r_\pi$, $r_0$) of $Q_1$.
   c) [5 pt] What is the small-signal gain of the amplifier?
   d) [5 pt] What is the input resistance?
   e) [5 pt] If we take into account the finite base currents in $Q_2$ and $Q_3$, what would be the collector current in $Q_1$? What is the percentage error introduced in Part c)?



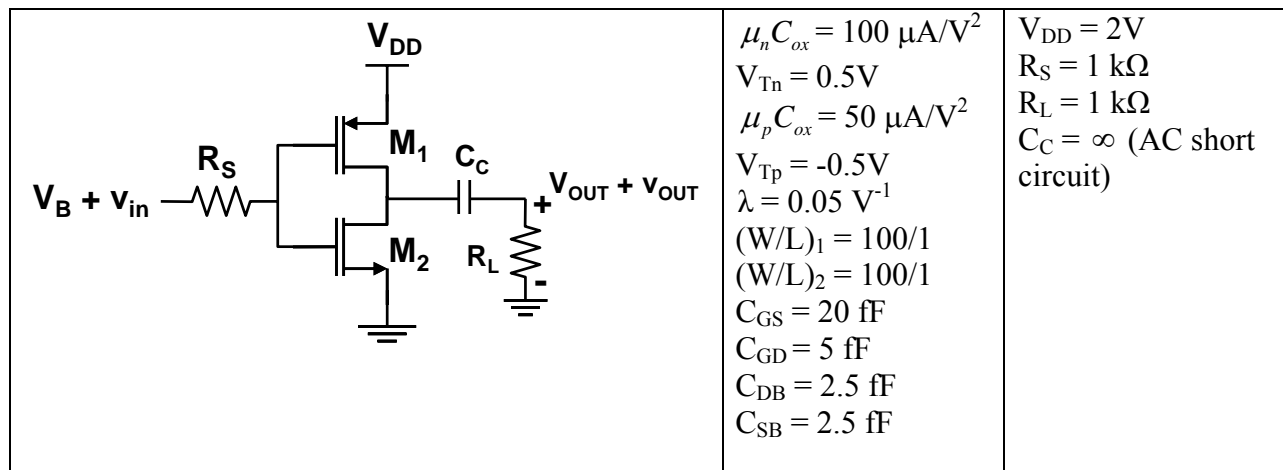| | BJT Parameters | $I_{REF}$ = 100 μA |
|---|---|---|
| | $I_{S,3}$ = $10^{-15}$ A | $R_S$ = 1 kΩ |
| | $A_{E,3}$ = 10 μm$^2$ | $R_E$ = 1 kΩ |
| | $A_{E,2}$ = 100 μm$^2$ | $R_L$ = 100 kΩ |
| | $V_A$ = 50V | $C_C$ = ∞ (AC short circuit) |
| | β = 100 | |
| | $C_\pi$ = 20 fF | |
| | $C_\mu$ = 5 fF | |
| | $C_{CS}$ = 10 fF | |

**(3)** Consider the amplifier below:
   a) [5 pt] Ignore the base current of BJTs, find the DC voltages at nodes X and Y.
   b) [5 pt] What is the emitter area ratio of $Q_2$ and $Q_3$? Calculate the emitter area of $Q_2$ if $I_{S,3} = 10^{-15}$ A and the emitter area of $Q_3$ is 2μm x 2μm.
   c) [5 pt] Find the output resistance of the amplifier.



| | $I_{REF} = 100\ \mu A$ | For MOS |
| --- | --- | --- |
| | $V_{CC} = 3$ V | $\mu_n C_{ox} = 100\ \mu A/V^2$ |
| | | $\mu_p C_{ox} = 50\ \mu A/V^2$ |
| | For all BJTs | $V_{Tn} = 0.5V$ |
| | $I_{S,3} = 10^{-15}$ A | $V_{Tp} = -0.5V$ |
| | $V_A = 10V$ | $\lambda = 0.05\ V^{-1}$ |
| | $\beta = 100$ | |
| | | $(W/L)_4 = 256/1$ |
| | | $(W/L)_5 = 64/1$ |
| | | $(W/L)_6 = 64/1$ |
| | | $(W/L)_7 = 16/1$ |

**(4)** Consider the following circuit:
   a) [5 pt] Calculate the DC bias voltage, $V_B$, such that the DC voltage of the output node is 1V. You need to include channel length modulation in your calculation.
   b) [5 pt] Under the DC bias condition, calculate the small-signal voltage gain of the amplifier.
   c) [5 pt] Find the input and output pole frequencies. What is the 3-dB frequency of this amplifier (in Hz)?



| $\mu_n C_{ox} = 100\ \mu A/V^2$ | $V_{DD} = 2V$ |
| --- | --- |
| $V_{Tn} = 0.5V$ | $R_S = 1\ k\Omega$ |
| $\mu_p C_{ox} = 50\ \mu A/V^2$ | $R_L = 1\ k\Omega$ |
| $V_{Tp} = -0.5V$ | $C_C = \infty$ (AC short circuit) |
| $\lambda = 0.05\ V^{-1}$ | |
| $(W/L)_1 = 100/1$ | |
| $(W/L)_2 = 100/1$ | |
| $C_{GS} = 20$ fF | |
| $C_{GD} = 5$ fF | |
| $C_{DB} = 2.5$ fF | |
| $C_{SB} = 2.5$ fF | |

**(5)** The following is a CMOS 2-stage amplifier:
  a) [3 pt] Find the DC bias currents in $M_1$ and $M_3$.
  b) [6 pt] Find the small-signal voltage gain and the output impedance of the amplifier $(R_L = \infty)$.
  c) [3 pt] For $R_L = 100$ k$\Omega$, find the maximum and minimum output voltages with all transistors in saturation.
  d) [3 pt] For $R_L = 100$ $\Omega$, find the maximum and minimum output voltages with all transistors in saturation.



$V_{DD} = 3$V
$I_{BIAS} = 100$ $\mu$A
$\mu_n C_{ox} = 100$ $\mu$A/V$^2$ , $V_{Tn} = 0.5$V
$\mu_p C_{ox} = 50$ $\mu$A/V$^2$ , $V_{Tp} = -0.5$V
$\lambda = 0.05$ V$^{-1}$
$(W/L)_1 = 20/1$ ($\mu$m/$\mu$m)
$(W/L)_2 = 20/1$ ($\mu$m/$\mu$m)
$(W/L)_3 = 100/1$ ($\mu$m/$\mu$m)
$(W/L)_4 = 100/1$ ($\mu$m/$\mu$m)
$(W/L)_5 = 10/1$ ($\mu$m/$\mu$m)
$(W/L)_6 = 10/1$ ($\mu$m/$\mu$m)
$(W/L)_7 = 10/1$ ($\mu$m/$\mu$m)