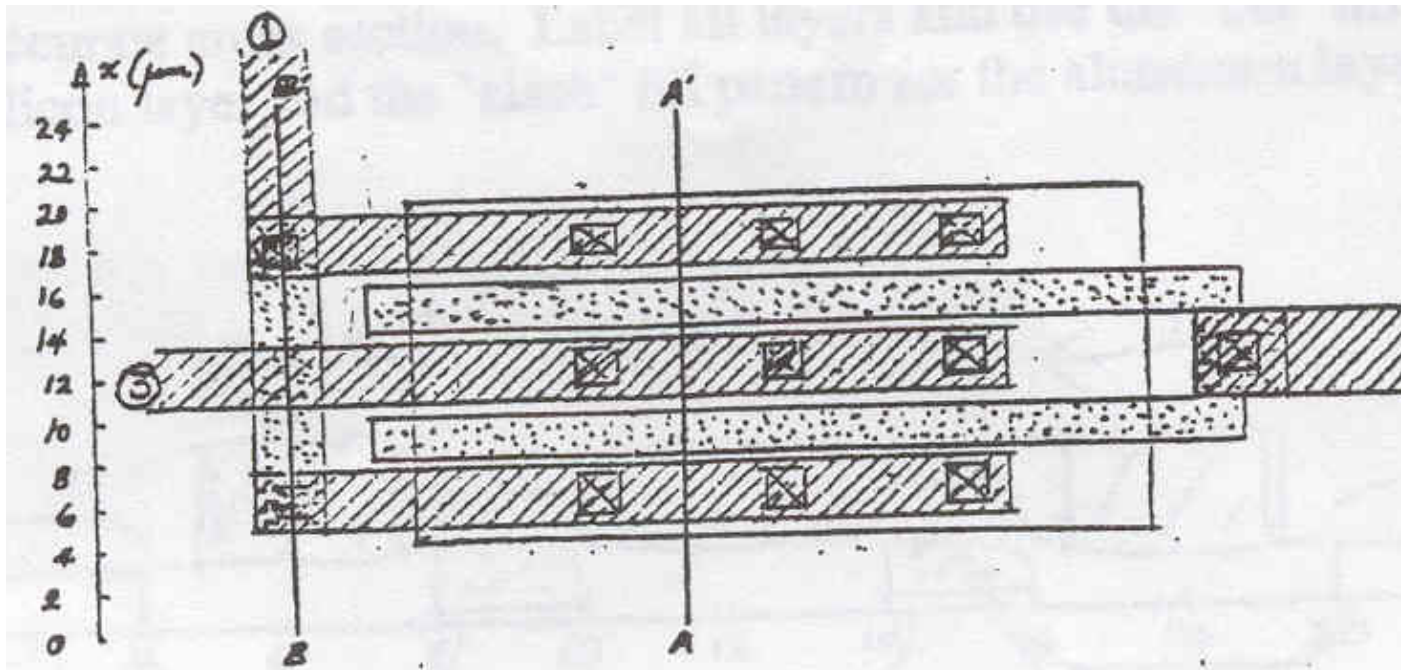Untitled Document

University of California at Berkeley
College of Engineering
Department of Electrical Engineering
and Computer Sciences
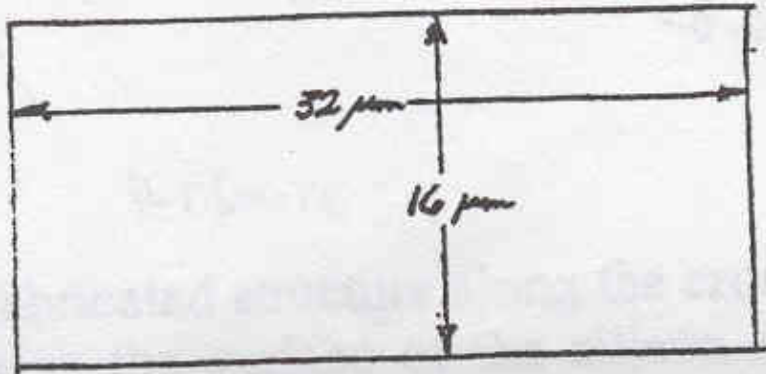
R.T. Howe, Fall 1997
EECS 105
Midterm I: October 8, 1997

· Closed book and notes; one 8.5" X 11 "formula sheet (both sides)
· Do all work on exam pages
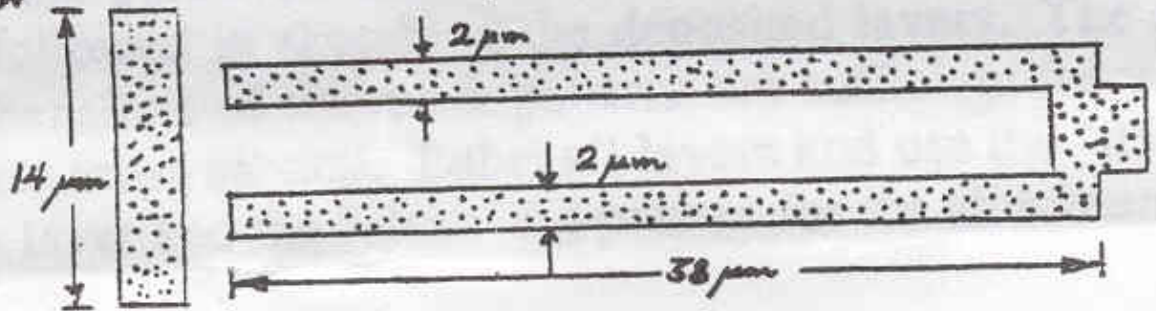· You have 80 minutes; use your time wisely!
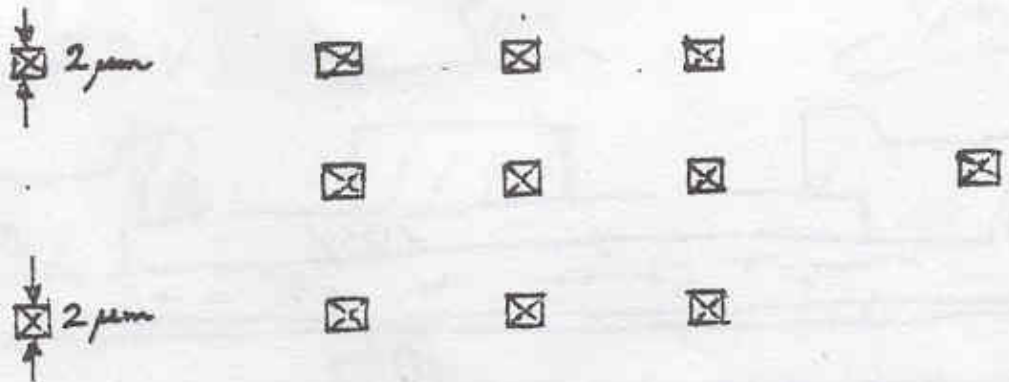
Problem #1 MOSFET LAYOUT [18 points]

OXIDE MASK
(DARK FIELD)

POLYSILICON
MASK
(CLEAR
FIELD)

CONTACT
MASK
(DARK FIELD)

METAL
MASK

Process Flow:

0. Starting material: p-type silicon wafer

1. Grow 0.5 um of thermal SiO2 and pattern using the **oxide mask**.

2. Grow 250 A = 0.025 um of thermal SiO2 for the gate oxide.

3. Deposit 0.5 um of n+ polysilicon and pattern using the **polysilicon mask**.

4. Implant arsenic (dose $Q_a = 10^{13}$ cm^{-2}) and anneal to obtain a junction depth $x_j = 0.5$ um. The arsenic does not penetrate the 0.5 um-thick oxide.

5. Deposit 0.5 um of CVD SiO2 and pattern using the **contact mask**.

6. Deposit 1 um of aluminum and pattern using the **metal mask**.

a) [7 pts.] Accurately sketch the fabricated structure along the cross section A-A'. Use the horizontal line below as the surface of the silicon wafer. The vertical scale on should be followed in sketching the deposited layers. The x axis on the layout and the dimensions of the mask patterns are sufficient for you to have a reasonably accurate cross section. Label all layers and use the "dot" fill pattern for the polysilicon layer and the "slash" fill pattern for the aluminum layer.

surface ———————————————————————————— x

b) [7 pts.] Accurately sketch the fabricated structure along the cross section B-B'. Use the horizontal line below as the surface of the silicon wafer. The vertical scale should be followed in sketching the deposited layers. The x axis on the layout and the dimensions of the mask patterns are sufficient for you to have a reasonably accurate cross section. Label all layers and use the "dot" fill pattern for the polysilicon layer and the "slash" fill pattern for the aluminum layer.

surface — *x*

c) [4 pts.] There are three metal interconnections to this device, which are labeled "1", "2", and "3" on the layout. Draw the schematic for this device, including the symbol (or symbols) for the MOSFET (or MOSFETs) located between "1", "2", and "3". Be sure to indicate the (W / L) ratios for the transistor or transistors.

Problem #2 NEW MOS INVERTER LOAD [17 points]

A new non-linear resistive element has a current-voltage characteristic given by:

$$I\text{sup} = (1/5\ \text{kilo-Ohms})*(V\text{sup}/1\ \text{Volt})^{(1/2)}$$

a) [3 pts.] Plot Isup as a function of Vsup on the graph below. Your plot should be accurate for Vsup = 0, 1, and 4V.

Isup [uA]

Vsup [V]

b) [4 pts.] Find the numerical value of the small-signal resistance r at the operating point $Vsup=4V$.

c) [6 pts.J We now use the resistive element as the load in an inverter. Using the load-line technique on the Id $=Isup$ versus $Vout$ graph, sketch the transfer curve $Vout$ versus Vin on the graph below. You should have intersection points for input voltages $Vin= 0, 1, 2, 2.5, 3,$ and 4 V.
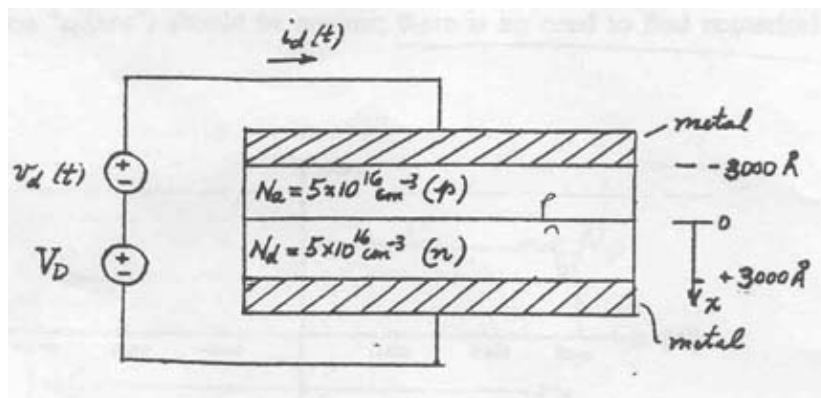
Given: $MUnCox = 50$ uA/V^2, $Vtn = 1$ V, $(W/L) = 4/2 = 2$, and $LAMBDAn = 0$

Vdd = 5 V

Vout (4 um / 2 um)

+
Vin
-

Vout [V]

Id, Isup [uA]

Vout [V]
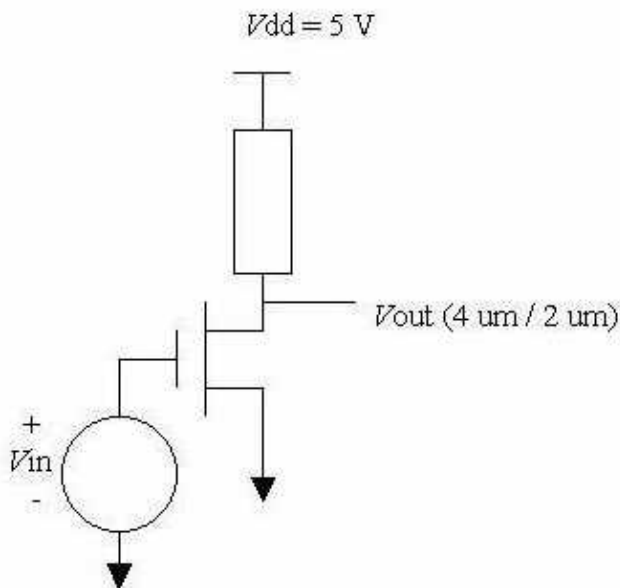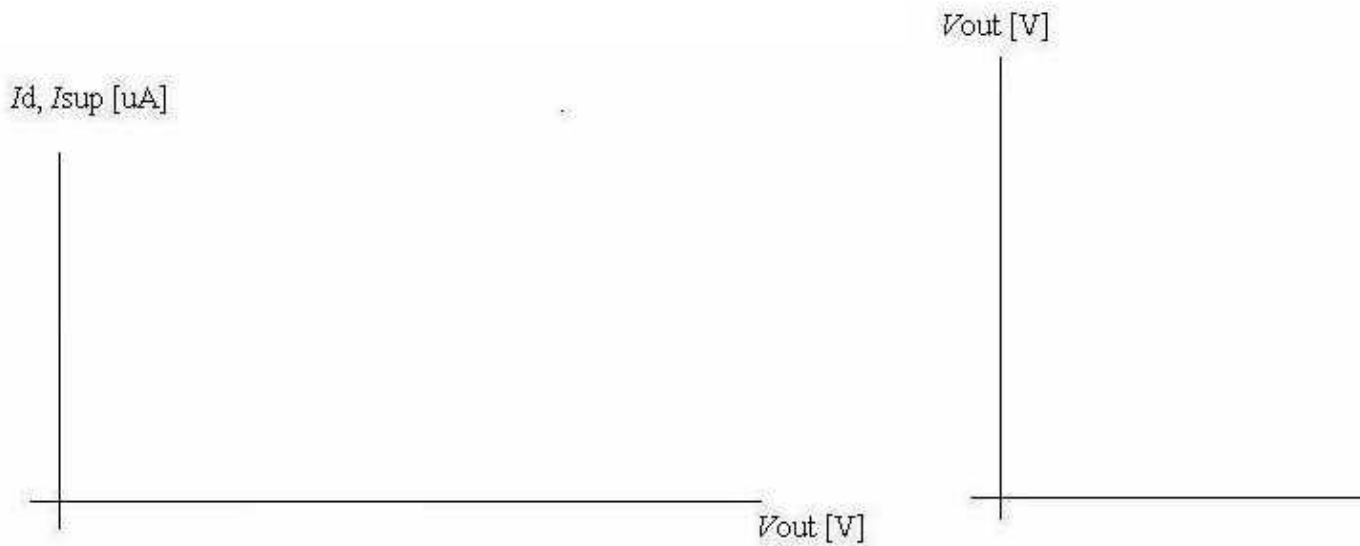
d) [4 pts.] Find the numerical value of the slope A_v of the transfer curve found in part (c) at $Vin = 2.5$ V. Given: the MOSFET is saturated for this value of Vin. Note: it is not necessary to solve part (c) to answer this part.
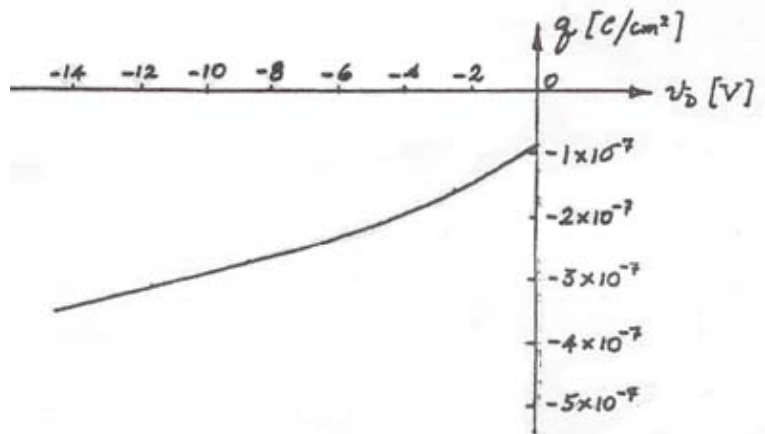
Problem #3 Metal/p/n/Metal Capacitor [15 points]

$i_d(t)$

metal

$- -3000 \, \text{Å}$

$v_d(t)$

$N_a = 5 \times 10^{16} \, \text{cm}^{-3} \, (p)$

ρ

V_D

$N_d = 5 \times 10^{16} \, \text{cm}^{-3} \, (n)$

0

$+3000 \, \text{Å}$

x

metal

Given: $q = 1.6 \times 10^{-19}$ C, $EPSILONs = 1.04 \times 10^{-12}$ F/cm, 1 Å $= 10^{-8}$ cm; 1 um $= 10^{-4}$ cm

a) [4 pts.] From the plot of charge stored (on the p-side of the junction) versus the diode voltage below, the

charge for $Vd = 0$ V is -8×10^{-8} cm-2. What is the overall depletion width Xdo for this case?

b) [4 pts.] Sketch the capacitance (units: F/cm2) versus diode voltage for this metal/p/n/metal structure on the graph below.

Given: $Xd = 4000$ A for $Vd = -2.4$ V and $Xd = 6000$ A for $Vd = -6.4$ V

If you couldn't solve part (a), you can assume without loss of credit that $Xdo = 1500$ A for $Vd = 0$ V (... not the correct answer to (a), of course). Your plot should be accurate at these voltages.
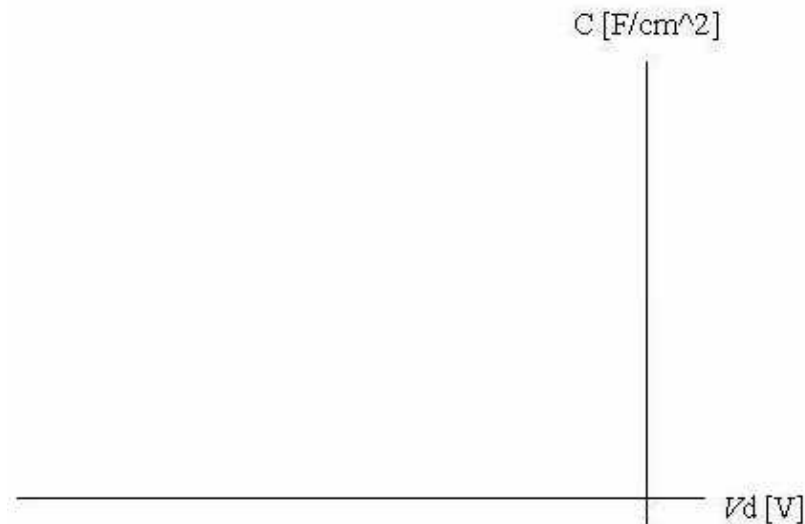
c) [4 pts.] Sketch the charge density $RO(x)$ through the structure for $Vd = -10$ V on the graph below. The relative magnitude of the densities and any sheet charges (shown as delta function "spikes") should be correct; there is no need to find numerical values.

$\rho(x)$
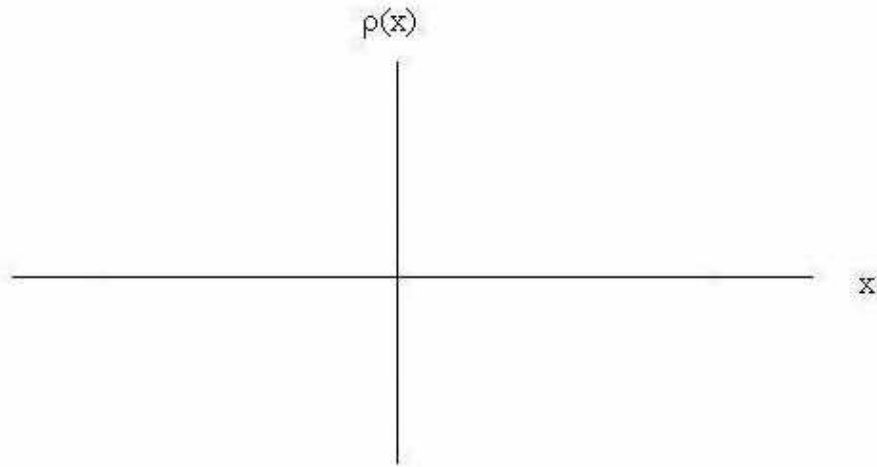
d) [3 pts.] For the case where the small-signal voltage is $Vd(t) = 5$ mV $\sin(2pi*10^6*t)$ and the DC bias is Vd = -10 V, find the small-signal current $Id(t)$ into the structure. Given: the area of the structure is 400 um^2.