UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 105: Microelectronic Devices and Circuits   Fall 2010

Final Examination
Time allotted: 120 minutes

NAME: _____   _____

STUDENT ID#:   _____

INSTRUCTIONS:
1. **SHOW YOUR WORK. (Make your methods clear to the grader!)**
2. **Clearly mark (underline or box) your answers.**
3. **Specify the units on answers whenever appropriate.**

SCORE: 1 _____ / 20

2 _____ / 20

3 _____ / 20

4 _____ / 20

Total   _____ / 80

PHYSICAL CONSTANTS

Description	Symbol	Value
Electronic charge	q	1.6×10^{-19} C
Boltzmann's constant	k	8.62×10^{-5} eV/K
Thermal voltage at 300K	$V_T = kT/q$	0.026 V

PROPERTIES OF SILICON AT 300K

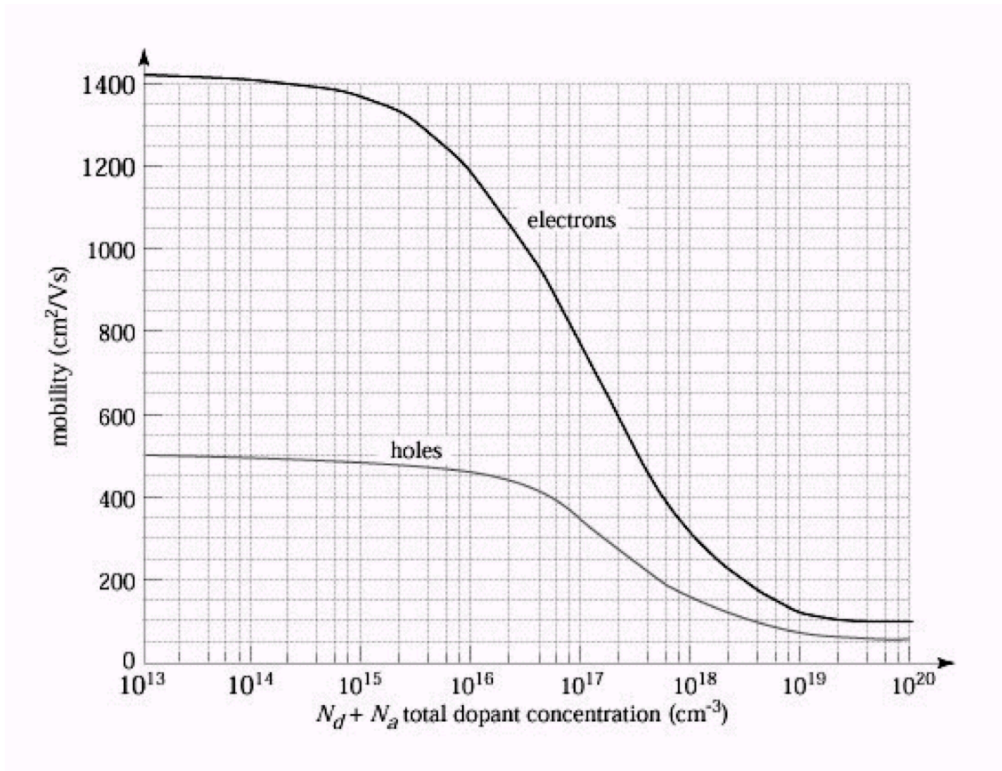| Description	Symbol	Value
Band gap energy	E_G	1.12 eV
Intrinsic carrier concentration	n_i	10^{10} cm^{-3}
Dielectric permittivity	ε_{Si}	1.0×10^{-12} F/cm

USEFUL NUMBERS

$V_T \ln(10) = 0.060$ V at T=300K
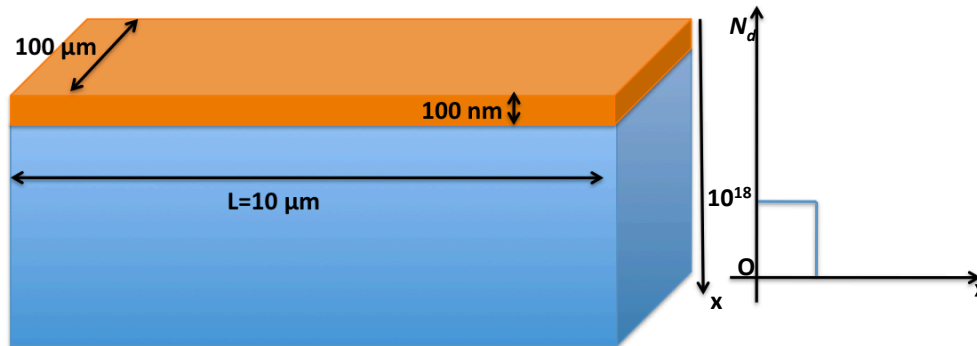
$\exp(30) \sim 10^{13}$

Depletion region Width:

$$W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)\left(V_{bi}-V_{Applied}\right)}$$

Electron and Hole Mobilities in Silicon at 300K

Prob 1: [20 pts]

(a) Consider a Si slab whose length is 10 μm and width is 100 μm. Assume that the this slab is doped with $N_d = 10^{18}$ cm^{-3} uniformly upto a depth of 100 nm starting from the surface as shown in the following Figure.

(i) [8 pts] Do you expect a depletion region at the interface of doped and undoped region? If yes, i. Describe how it forms ii. What the built-in voltage will be and iii. What the width of the depletion region will be at equilibrium. If there should not be any depletion region, explain why. Assume T=300K.

(b) [6 pts] For the slab as described in prob (a) find out the current that will flow if a voltage of V=1 V is applied along the length of the slab. Clearly write down all the approximations made.

(c)[6 pts] Why is there an electric field in a p-n junction? How does the electric field change for forward and reverse bias as compared to zero bias? Qualitatively explain the reason for dominant transport mechanism (drift, diffusion etc) in the forward and reverse bias starting from how the electric field changes as a function of bias.

Prob 2. [20 pts]

    (a) [5 pts] Starting from the fact that Current is a product of charge density per square area velocity and the width of the device, derive an expression for saturation current in a MSOFET dominated by velocity saturation.

(b) [5 pts] Looking at the Drain current vs. Drain voltage characteristics, it is possible to determine if the MOSFET is dominated by velocity saturation. Explain how this could be done by drawing necessary diagrams.

(c) [5 pts] Draw the charge profile looking from the gate to the body of a n-channel (p body) MOSFET at the accumulation and inversion region. Clearly indicate all the different regions (gate metal, oxide, semiconductor etc.) in your diagrams.

(d) [5 pts] If the total input capacitance (considering for C_μ, C_π etc.) is the same for a CE and a CS stage, which one is expected to have a higher cutoff frequency? Why? You may ignore input resistances in your analysis.

Prob 3. [20 pts]

    (a) [10 pts] Assume that for a particular application, one needs to design a circuit that will have a gain of -100. However, the load resistance is such that $|g_mR_L|$=10. How would you design the circuit so that the specification can be made? Draw the circuit and find out an expression for its voltage gain.

(b) [10 pts]

    (i)   Find out the voltage gain for the following circuit (assume ß>>1). Your answer should be numeric. Assume both transistors are identical and ignore early effect.

V_{cc}

V_{in}

Q_1

V_{out}

Q_2
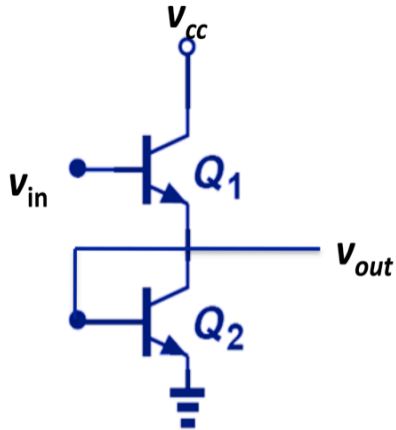
    (ii)   What will be the gain if the circuit is modified as follows (assume ß>>1). Your answer should be numeric. Assume both transistors are identical and ignore early effect.

V_{cc}

Q_1

V_{out}

V_{in} Q_2

8
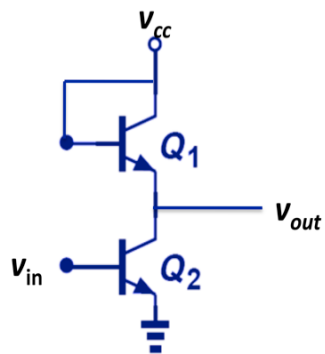
Prob 4. [20 pts]

   (a) [4 pts] Assume that for a particular application, one needs to copy a Reference current
      100 times. If you have flexibility to use either BJT or MOSFET based current mirrors,
      which one will you choose? Why?

   (b) [4 pts] Assume that there is supply noise in a differential amplifier. Answer the following
      questions by writing **yes** or **no** in the table:

If there is variation in	Differential output will be noisy
Tail current	
Collector Resistance	
ß	
Early voltage	

(c) [4 pts] Find out the differential voltage gain of the following circuit. Assume $\lambda=0$.
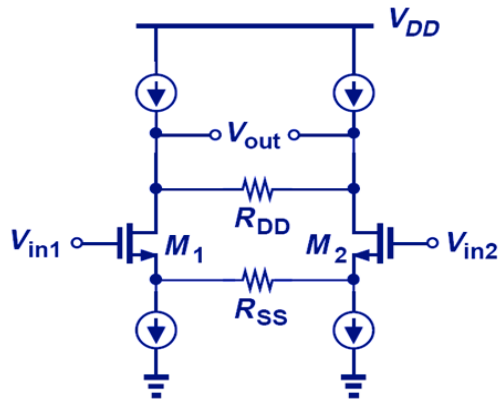
(d) [8 pts] One needs to design a differential amplifier which will have a single ended output. However, for this design, an ideal tail current source is not available and can only be obtained by copying a golden current (a reference current) which is flowing *from* the supply rail.

(i)   [3 pts] In a schematic diagram describe how this circuit can be designed.

(ii)   [5 pts] Draw the actual circuit to perform this task.