Microelectronic Devices and Circuits- EECS105
Final Exam

Wednesday, December 13, 2000

Costas J. Spanos
University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

Your Name: ____
(last) *(first)*

Your Signature: ____

1. *Print and sign your name on this page before you start.*
2. *You are allowed three, 8.5"x11" handwritten sheets. No books or notes!*
3. *Do everything on this exam, and make your methods as clear as possible.*

Problem 1	________	/ 24
Problem 2	________	/ 26
Problem 3	________	/ 26
Problem 4	________	/ 24
TOTAL	_________	/ 100

MOS Device Data (you may not have to use all of these...)

$\mu_n C_{ox} = 50\mu A/V^2$, $\mu_p C_{ox} = 25\mu A/V^2$, $V_{Tn} = -V_{Tp} = 1V$, Lmin = 2μm. $V_{BS} = 0$.
$\lambda_n = \lambda_p = 0.1V^{-1}$ when L = 1μm, and it is otherwise proportional to 1/L
$C_{ox} = 2.3fF/\mu m^2$, $C_{jn} = 0.1fF/\mu m^2$, $C_{jp} = 0.3fF/\mu m^2$, $C_{jswn} = 0.5fF/\mu m$,
$C_{jswp} = 0.35fF/\mu m$, $C_{ovn} = 0.5fF/\mu m$, $C_{ovp} = 0.5fF/\mu m$

Problem 1 of 4: Answer each question briefly and clearly. (4 points each, total 24)

Why are bipolar transistors capable of providing more drive current compared to MOS transistors that occupy similar area? (give a qualitative answer)

Comparing a Common Collector to a Common Drain voltage buffer amplifier, one sees some advantages and disadvantages. Place a mark below to indicate your choice, trying to get the largest DC voltage gain.

Aspect	CC	CD
Rin		
Rout		
Av		

In the IC industry "layout designers" can manipulate lateral device dimensions (L, W, area of base-emitter junction, etc.) while "process designers" manipulate vertical dimensions (Tox, base-width) and doping levels. List a parameter that each designer can change to affect the respective parameter, or write "none" if the designer cannot affect the value of the respective parameter:

Parameter	Layout Designer	Process Designer
V_{Tn}		
r_o (NMOS)		
g_m (NMOS)		
r_o (npn)		
g_m (npn)		
Cgs		

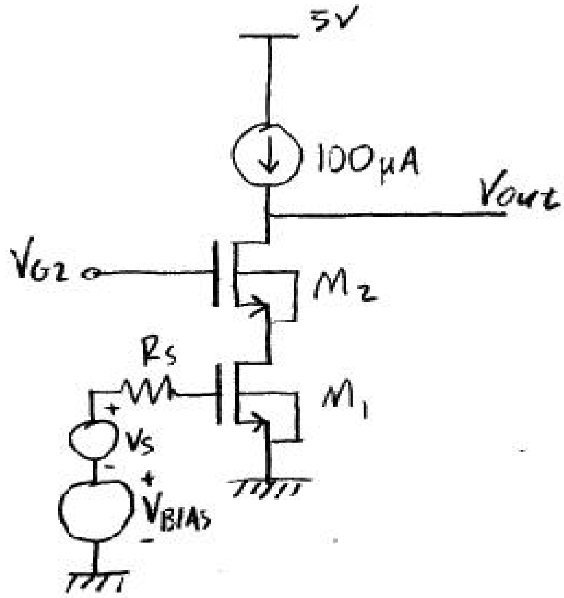
What advantage(s) does a casc**o**de configuration has over a casc**a**de configuration?

Which conditions must be satisfied so that the open circuit time constant method leads to an exact solution?

In your own words, how does the dreaded "Miller effect" limit frequency response of a high voltage gain amplifier?

Problem 2 of 4 (26 points)

Consider the following cascode amplifier, driven by a perfect current source ($r_{oc}=\infty$)



For each of the following questions, make sure that you show the expressions before you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!

a) Find $(W/L)_1$ *ratio* so that the *overall* Gm of this amp is 1mS. (Do not specify values for W and for L here. That comes later). (5 points)

Expression for $(W/L)_1$	Value
$(W/L)_1=$	

b) Assume that $g_{m2}=g_{m1}$, and $r_{o2} = r_{o1}$. Find the value of L_1 so that $r_{o1} = 200k\Omega$, and calculate the respective value of the overall Rout of this amplifier. (5 points)

Expression for L_1	Value
$L_1 =$	

Expression for Rout	Value
Rout =	

c) Find the open circuit voltage gain of this two stage amplifier ($r_{oc}=\infty$). (5 points)

Expression for Voltage Gain	Value	in db
vout/vin =		

d) Calculate V_{BIAS} (ignoring channel-length modulation). Assume that $(W/L)_1 = (W/L)_2 = 16$ (note that this is not the correct answer to question 2.a) (5 points)

Expression for V_{BIAS}	Value
V_{BIAS} =	

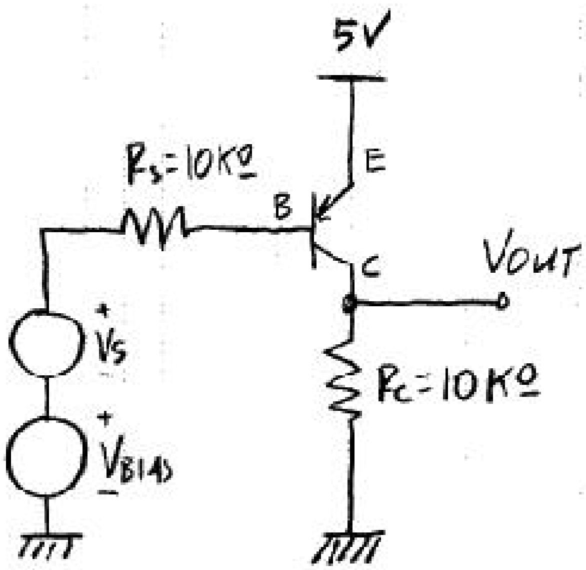
e) Assuming that $(W/L)_2 = 16$, find the value for V_{G2} that will give you the maximum voltage swing for this amp. Explain your thinking in one sentence (ignore channel length modulation).
(6 points)

What limits Vout min?

Expression for V_{G2}	Value
$V_{G2} =$	

Problem 3/4 (26 points)

Consider the following pnp CE amplifier. Note that $\beta o = 50$, $I_S = 10^{-17}$A and V_A = infinity. (Be very careful with signs in this problem!).



For each of the following questions, make sure that you show the expressions before you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!

a) Calculate V_{BIAS} so that Vout = 2.5V. Ignore I_B and Rs for this question. (Do NOT assume that V_{BE} is exactly -0.7V). (5 points)

Expression for V_{BIAS}	Value
V_{BIAS}=	

b) Find Rout and the voltage gain, if R_L = infinity. (8 points)

Expression for Rout	Value
Rout =	

Expression for Voltage Gain	Value
vout/vin =	

c) Calculate the value of R_L that will cut the gain by a factor of two. (Assume that R_L is connected through a small coupling capacitor, so that it does not disrupt the biasing of the transistor.) (5 points)

Expression for R_L that cuts the gain by a factor of 2.	Value
R_L =	

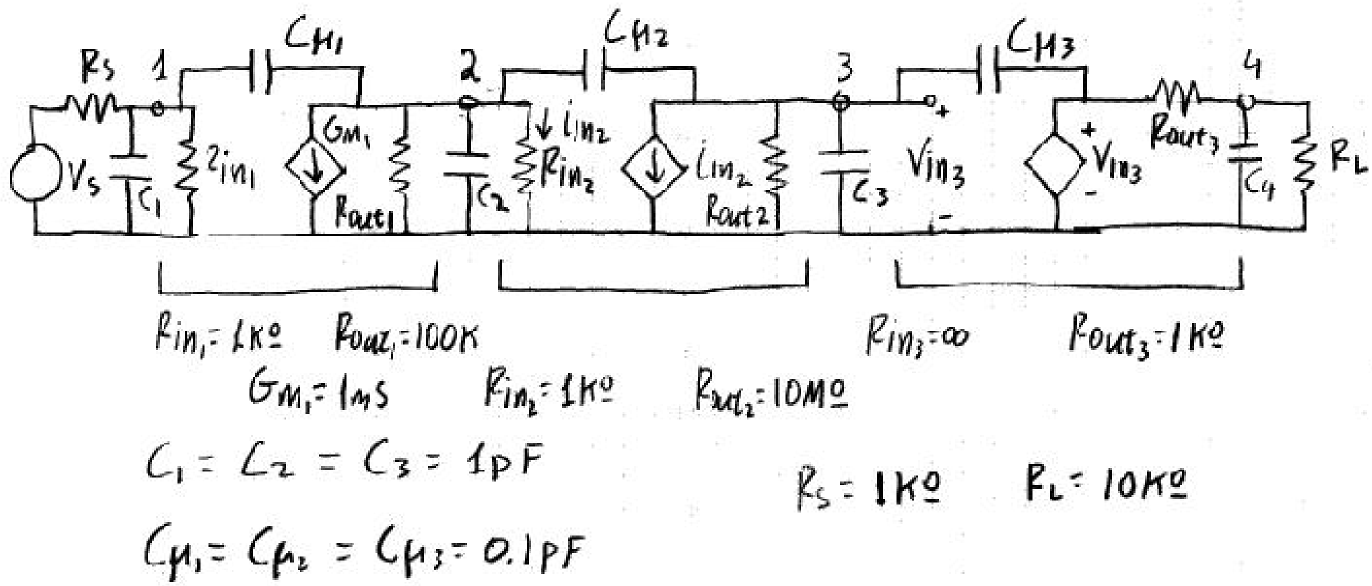
d) If you could increase βo, how much would you have to increase it in order to increase the gain by 10%. (Hint: assume that the new, improved $\beta o' = X\beta o$, and write an expression that you can use to calculate the value of the factor X). (8 points)

Expression for X (multiplier for increasing βo.)	Value
X =	

Problem 4/4 (24 points)

The following is a cascade of three 2-ports: a transconductance amplifier, a current buffer and a voltage buffer. The aim of this circuit is to produce lots of voltage gain over a wide bandwidth.

.



a) Find the low frequency voltage gain vout/vin. (this means that you can ignore all the capacitors). Do this in stages as shown in the table below: (6 points)

Expression	Value
$v_2/v_s =$	
$v_3/v_2 =$	
$v_{out}/v_3 =$	
$v_{out}/v_s =$	

b) Replace all "cross-over" caps $C_{\mu 1}$, $C_{\mu 2}$, $C_{\mu 3}$, with their Miller equivalent C_{M1}, C_{M2}, C_{M3}.
(6 points)

Expression	Value
C_{M1} =	
C_{M2} =	
C_{M3} =	

c) Calculate the Open Circuit Time Constant for the nodes 1, 2, 3 and 4. (6 points)

Expression	RC	Value
R_{T1} =	RC_1=	
R_{T2}=	RC_2=	
R_{T3}=	RC_3=	
R_{T4}=	RC_4=	
Total		

d) Calculate the ω_{3db} of this amp (6 points)

Expression for ω_{3db}.	Value
ω_{3db} =	

~ That's All Folks! ~