**EECS 100** **Fall 1999** **Midterm # 2**

## NAME:

## ID #:

| # 1 | # 2 | # 3 | # 4 | # 5 | # 6 | TOTAL |
|---|---|---|---|---|---|---|
| 12 | 18 | 15 | 15 | 15 | 15 | 90 |

**Instructions:**

1 Write your name and student ID number.

2 Read the questions carefully.

3 Write your solution clearly.

4 This exam has 6 questions worth 90 points, so you should proceed at approximately 1 point per minute.

**Problem # 1** $(2+2+2+2+1+3=12$ points)

Convert the following sinusoids to phasors.

(a) $3\cos(\omega t)+4\sin(\omega t)$

(b) $\sqrt{2}\sin(\omega t-45^{\circ})$

Convert the following phasors to sinusoids. Assume the frequency is $\omega$.

(d) $3+4j$

(e) $5\exp(j\pi/2)$

Number conversions.

(c) Write the binary number 1111 in decimal.

(d) Write the decimal number 1111 in binary.

**Problem # 2** $(3+3+3+3+3+3 = 18$ points)

(a) List three features of digital electronics that make its use attractive.

(b) An inexpensive low pass filter can be built using an inductor or using a capacitor. Which is preferable? Why?

(c) The (Kanji) Chinese alphabet has 3000 characters. How many 8-bit bytes are needed to represent one Chinese character?

(d) English text is to be transmitted by modem on a serial binary line. Each character is encoded in ASCII using 1 eight bit byte. The maximum transmission rate is 56 Kilo baud. How many seconds does it take to transmit one page consisting of 700 English characters?

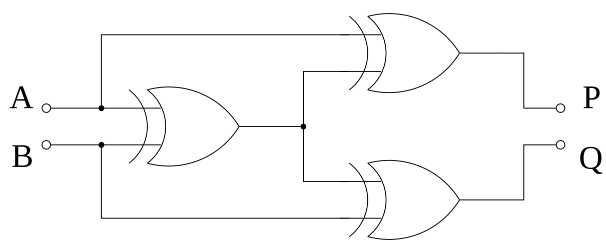
(e) You want to build a digital speedometer capable of measuring speeds in the range from $-30$ mph to 150 mph. Your digital speedometer can have a quantization error of $\pm 0.25$ mph. How may binary lines are needed in the output data bus of the digital speedometer?

(f) What are the units of capacitance in MKS (meter-kilogram-second-coulomb) units?

**Problem # 3** (7+7+1 = 15 points)

(a) Build a **NOR** gate using at most 4 **NAND** gates.

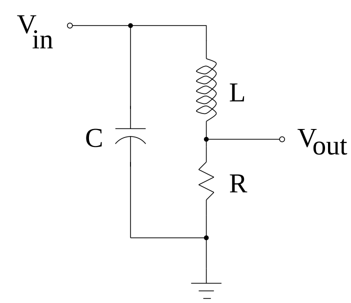
(b) For the logic circuit shown below, fill out the truth-table.
What does this circuit do ?



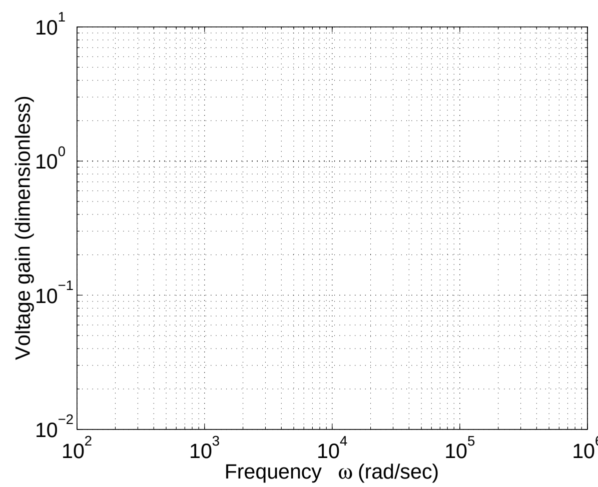

| A | B | P | Q |
|---|---|---|---|
| 0 | 0 | | |
| 0 | 1 | | |
| 1 | 0 | | |
| 1 | 1 | | |

**Problem # 4** (4+8+1+2 = 15 points)

(a) Consider the circuit shown across. Let $\mathbb{V}_{in}$ and $\mathbb{V}_{out}$ be the phasors of the input voltage $V_{in}$ and the output voltage $V_{out}$ respectively. Find $\mathbb{V}_{out}$ in terms of $R, L, C, \omega$ and $\mathbb{V}_{in}$.




(b) With $R = 1$ **KΩ**, $L = 100$ **mH**, $C = 3$ $\mu$**F**, sketch the frequency response of the voltage magnitude gain from $\mathbb{V}_{in}$ to $\mathbb{V}_{out}$. Use the log-log scale graph-paper supplied below.



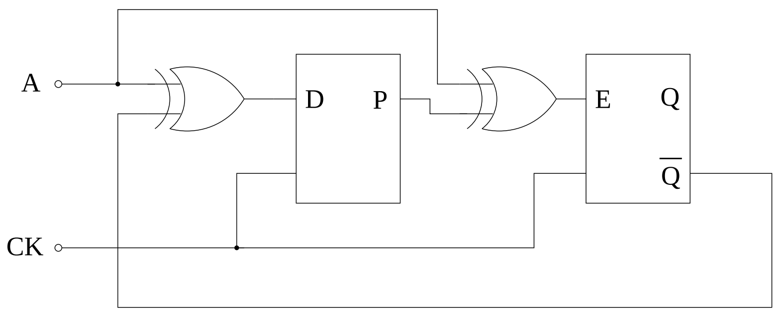

(c) Is this a low-pass, band-pass, or high-pass filter ?

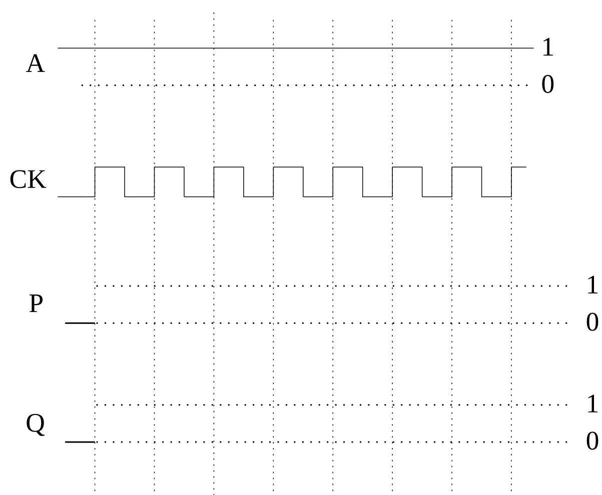
(d) Find the 3$db$ bandwidth of the filter.

**Problem # 5** (15 points)

Draw the timing diagram for the circuit shown below. Here, both flip-flops are D-type and trigger on the rising edge of the clock. Note that (as discussed in class) because of propagation delays, when a flip-flop triggers, the data signal *immediately* before triggering is transferred to the flip-flop output.

Hint: Note that $\mathbf{A = 1}$ always. Now, figure out what **D** and **E** are in terms of **P** and **Q**.



**Problem # 6** (15 points)

In this problem, you are asked to design a digital circuit. There is serial binary data arriving at **A**. You have to build a circuit that detects the presence of *three consecutive zeros* on this serial line. Anytime you get three consecutive zeros at **A**, the output of your circuit **F** equals **1**, and is held until the next bit arrives at **A**.

A sample timing diagram of how this circuit should behave is shown below.

You can use three D-type flip-flops and logic gates. There is also available a clock **CK** that is synchronized with the bit arrivals on the serial line **A**.