SID: _____

University of California, Berkeley – College of Engineering

Department of Electrical Engineering and Computer Sciences

Spring 2015 Instructors: Krste Asanović, Vladimir Stojanovic 2015-04-09

After the exam, indicate on the line above where you fall in the emotion spectrum between "sad" & "smiley"...

Last Name	**ANSWER KEY**
First Name	
Student ID Number	
CS61C Login	**cs61c-**
*The name of your **SECTION** TA (please circle)*	David | Donggyu | Fred | Jeffrey | Martin Nolan | Sagar | Shreyas | William
Name of the person to your Left	
Name of the person to your Right	
*All the work is my own. I had no prior knowledge of the exam contents nor will I share the contents with others in CS61C who have not taken it yet. **(please sign)***	

Instructions (Read Me!)

- This booklet contains 7 numbered pages including the cover page. **The back of each page is blank and can be used for scratch-work, but will not be looked at for grading.** (i.e. the sides of pages without the printed "SID: _____" header will not even be scanned into gradescope).
- Please turn off all cell phones, smartwatches, and other mobile devices. Remove all hats & headphones. Place your backpacks, laptops and jackets under your seat.
- You have 80 minutes to complete this exam. The exam is closed book; no computers, phones, or calculators are allowed. You may use two handwritten 8.5"x11" pages (front and back) of notes in addition to the provided green sheet.
- There may be partial credit for incomplete answers; write as much of the solution as you can. We will deduct points if your solution is far more complicated than necessary. When we provide a blank, please fit your answer within the space provided. "IEC format" refers to the mebi, tebi, etc prefixes.

	Q1	Q2	Q3	Q4	Q5	Q6	Total
Points Possible	8	13	8	6	4	6	45
Points Earned							

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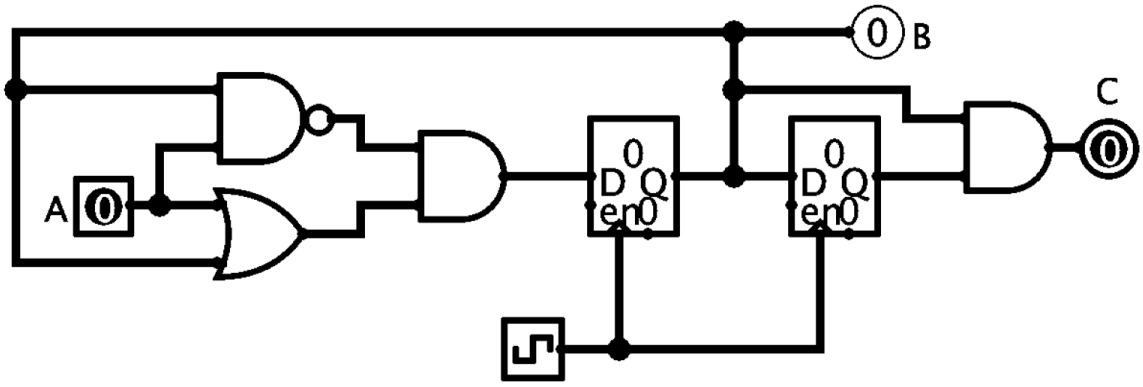
Q1: SDS (8 points)

You are given the following digital circuit. The registers have a setup time of 5ns, a hold time of 3ns, and a CLK-to-Q delay of 5ns, and all logic gates have a delay of 20ns. Assume inputs A and B are driven by registers with the same specifications.



a) What is the critical path delay, and what is the maximum clock frequency at which the circuit will operate correctly? You may leave answers as fractions.

(CLK-to-Q + CL + CL + setup) = 50 ns
1 / (50 ns) = 20 MHz

b) Someone meddles with the circuit, increasing the register hold time to 10ns and setting the clock rate to 1 Hz. Will the circuit still work after these changes? Explain your reasoning.

Hold time violation. CLK-to-Q < hold time so the second register will fail

c) What simplification could be made to this circuit to decrease the critical path delay without changing the exact sequence of outputs?

Replace the left combinational logic with a single XOR gate

Note that adding a register would change the exact sequence of outputs (delaying by one)

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Q2: Single-cycle Datapath and Control Logic (13 points)

Consider adding the following instruction to MIPS (disregard any existing definitions you may see on the green sheet):

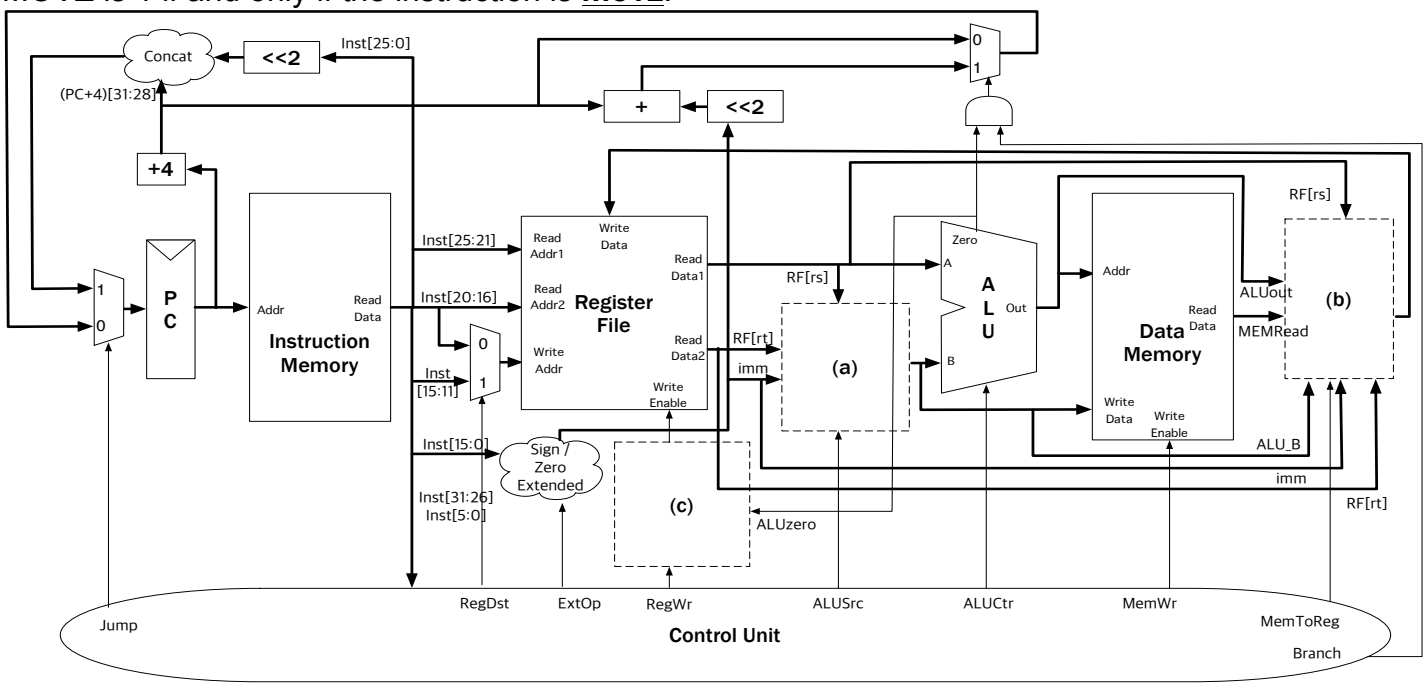
Instruction	Operation
movz rd, rs, rt	if (RF[rs] == 0) RF[rd] ← RF[rt]
movnz rd, rs, rt	if (RF[rs] != 0) RF[rd] ← RF[rt]

1. Translate the following C code using movz and movnz. Do not use branches.

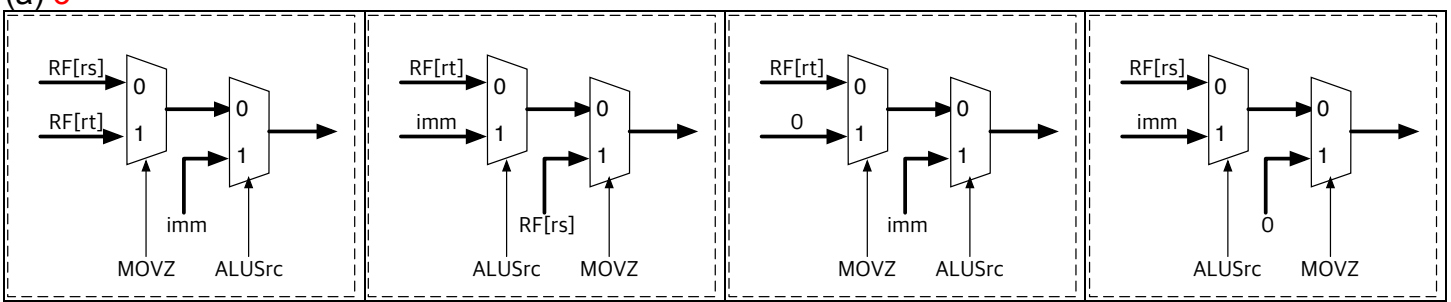
C code	MIPS

// a -> $s0, b-> $s1, c-> $s2
int a = b < c ? b : c;
	slt $t0, $s1, $s2
	movnz $s0, $t0, $s1
	movz $s0, $t0, $s2

2. Implement **movz** (but not movnz) in the datapath. Choose the correct implementation for (a), (b), and (c). Note that you do not need to use all the signals provided to each box, and the control signal MOVZ is 1 if and only if the instruction is **movz**.



(a) 3



1	2	3	4

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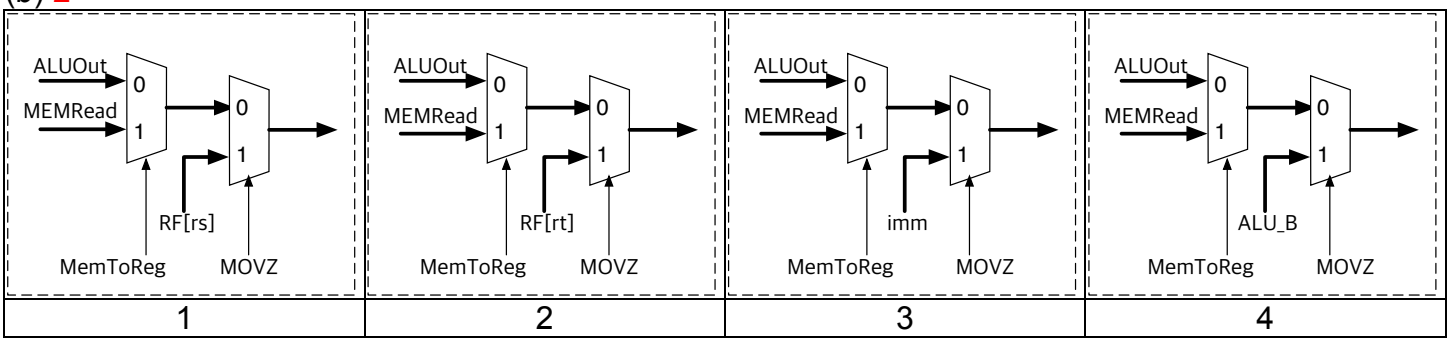
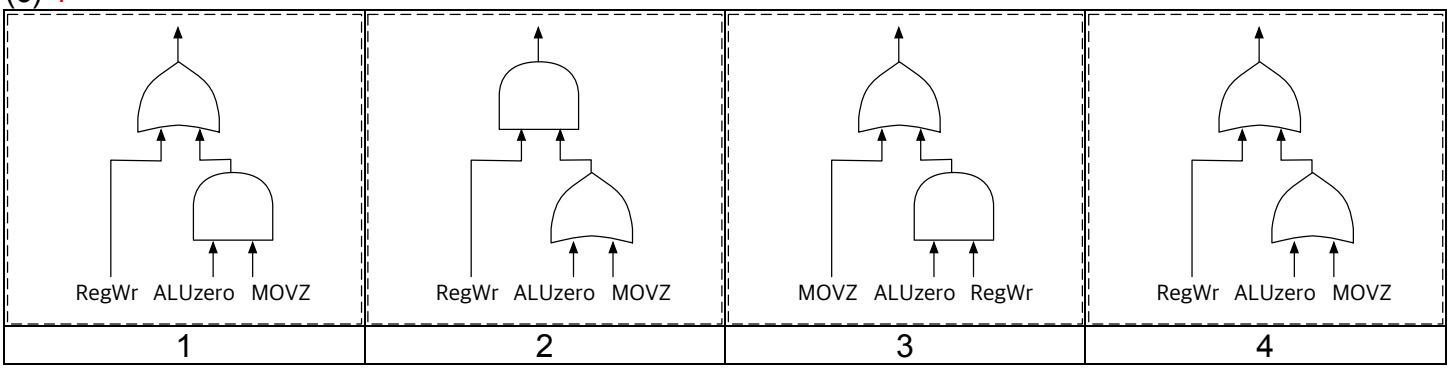
(b) 2



(c) 1



3. Generate the control signals for **movz**. The values should be 0, 1, or X (don't care) terms. You must use don't care terms where possible.

MOVZ	RegDst	ExpOp	RegWr	ALUSrc	ALUCtr	MEMWr	MemToReg	Jump	Branch
1	1	X	0	0	0001, 0010, or 0110	0	X	0	0

This table shows the ALUCtr values for each operation of the ALU:

Operation	AND	OR	ADD	SUB	SLT	NOR
ALUCtr	0000	0001	0010	0110	0111	1100

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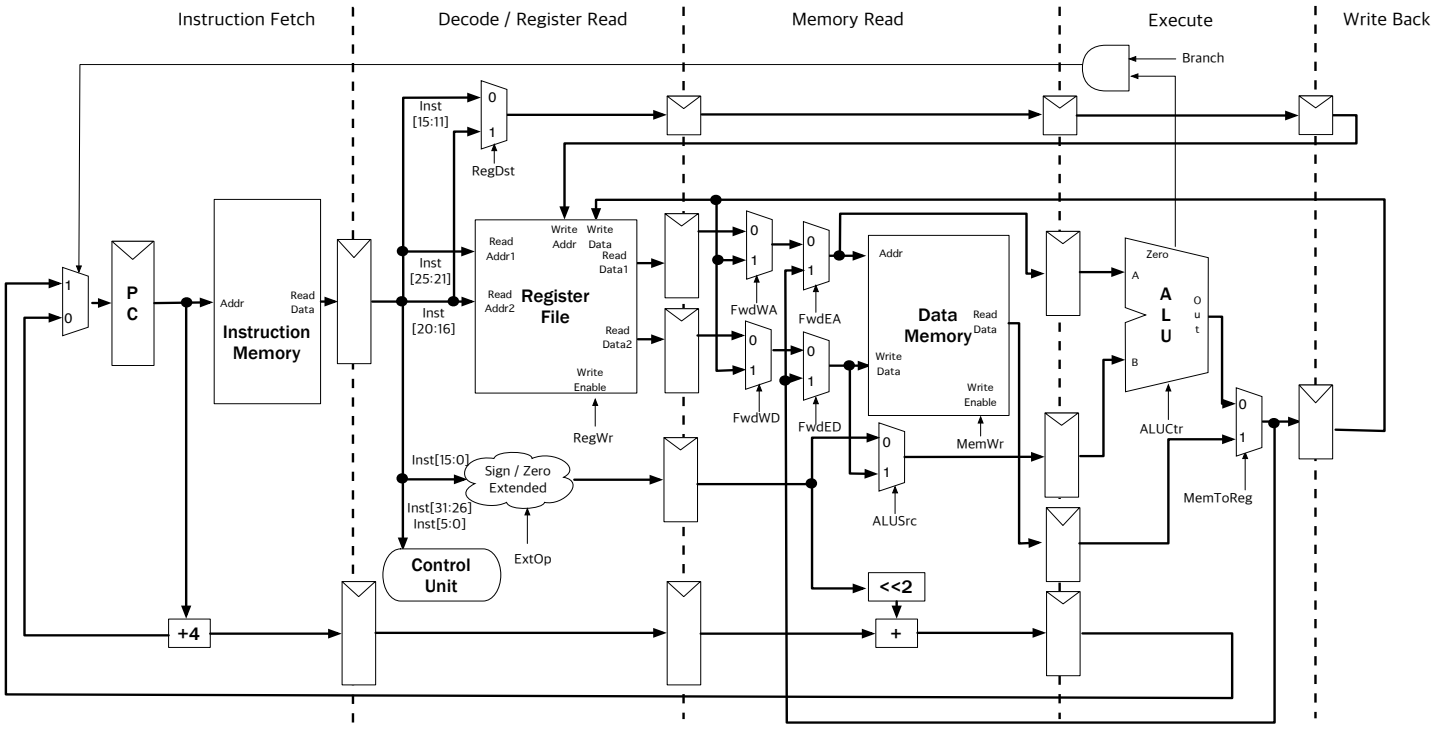
Q3: Pipeline Hazards (8 points)

We construct a different five-stage pipelined CPU by swapping the execute and the memory read stages. Note that there is now only indirect addressing for load word and store word.



a. Assume that this pipeline resolves control hazards by pipeline stalls. How many cycles is it stalled on a control hazard?

3 cycles

b. Should the pipeline stall for data hazards from load instructions? Give an example, fill in the corresponding pipeline stages, and explain your idea briefly in one or two sentences.
(F: Fetch, D: Instruction Decode, M: Memory, E: Execute, W: Write Back, B: Bubble)

Instructions	Cycles												
	1	2	3	4	5	6	7	8	9	10	11	12	13
`lw $t1, 0($t2)`	F	D	M	E	W								
`and $t3, $t1, $t2`		F	D	M	E	W							

No, the value of `$t1` are ready before the execute stage of the `and` instruction. We can forward its value to the next instruction from the pipeline registers without stalling the pipeline.

c. Give an example of a data hazard that will stall this pipeline, but not stall the original five-stage pipeline. Be as concise as possible.

```
add $t3, $t1, $t2
lw  $t1, 0($t3)
```

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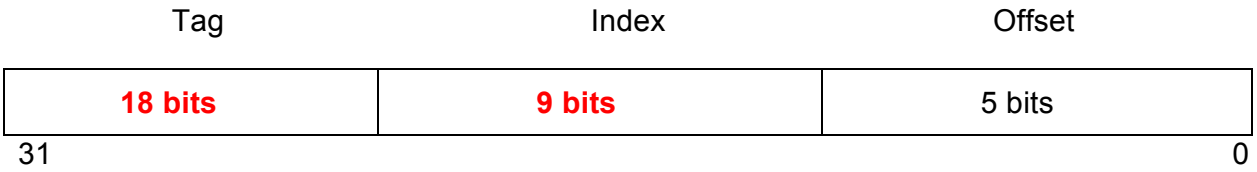
Q4: Cache Operations (6 points)

a) Consider a 32-bit physical memory space and a 32 KiB 2-way associative cache with LRU replacement. You are told the cache uses 5 bits for the offset field. Write in the number of bits in the tag and index fields in the figure below.



b) Assume the same cache as in part a).

```
int ARRAY_SIZE = 64 * 1024;
int arr[ARRAY_SIZE]; // *arr is aligned to a cache block

/* loop 1 */ for (int i = 0; i < ARRAY_SIZE; i += 8) arr[i] = i;
/* loop 2 */ for (int i = ARRAY_SIZE - 8; i >= 0; i -= 8) arr[i+1] = arr[i];
```

1. What is the hit rate of loop 1? What types of misses (of the 3 Cs), if any, occur as a result of loop 1?
   0% hit rate, Compulsory Misses

2. What is the hit rate of loop 2? What types of misses (of the 3 Cs), if any, occur as a result of loop 2?
   9/16 hit rate, Capacity Misses

Q5: AMAT (4 points)

Suppose you have the following system that consists of an:
L1$ with a local hit rate of 80% and a hit time of 2 cycles
L2$ with a global miss rate of 8% and a hit time of 15 cycles
DRAM accesses take 50 cycles

i. What is the AMAT of the L1 cache? _____

2 + 0.2 * (15 + 0.4 * 50) = 9

ii. Suppose we want to improve our AMAT, making sure that it is no greater than 6 cycles, by improving our L2$'s hit rate. What is the minimum possible local hit rate for L2$ that allows us to meet our AMAT requirement?

90%

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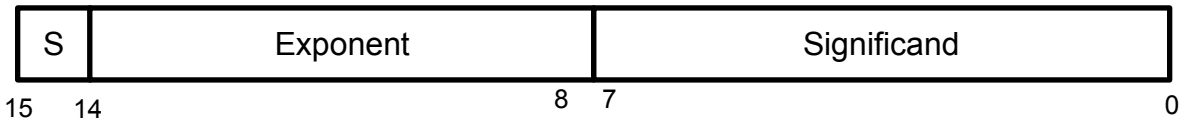
Q6: Floating Point (6 points)

We want to develop a new half-precision floating-point standard for 16-bit machines. The basic structure is as follows:



Here are the design choices:

- 1 bit for sign
- 7 bits for a signed exponent in 2's complement
- 8 bits for the significand
- Everything else follows the IEEE standard 754 for floating point, except in 16 bits.

In this new standard:

a) Convert the decimal number -10.625 to floating point. Write your answer in hexadecimal.

-1010.101
sign: 1
exponent: 3 -> 0x03
significand: 01010100 -> 0x54

0x8354

b) What is the smallest even number that is not representable? **2^10+2**

c) What is the smallest positive denormalized number? **2^-70 or 0x4001**