Your Name: ______________________________________

UNIVERSITY OF CALIFORNIA AT BERKELEY

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Department of Electrical Engineering
and Computer Sciences

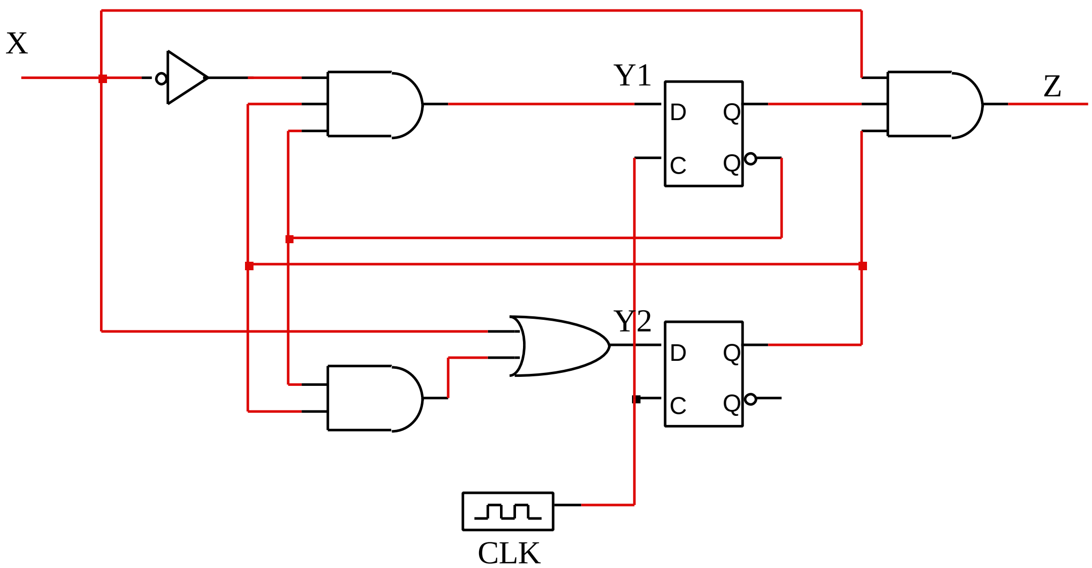
CS 150 - Spring 1994
Prof. A. R. Newton

Quiz 2

Room 145 Dwinelle, Tuesday 4/5
(Open Katz, Calculators OK, 1hr 20min)

Include all final answers in locations indicated on these pages. Use reverse side of sheets for all working. If necessary, attach additional sheets by staple at the end. BE SURE TO WRITE YOUR NAME ON EVERY SHEET.

(1) Consider the logic schematic diagram shown below:



(a) Is this a **Moore or Mealy** machine? ___Mealy__ (2pts)

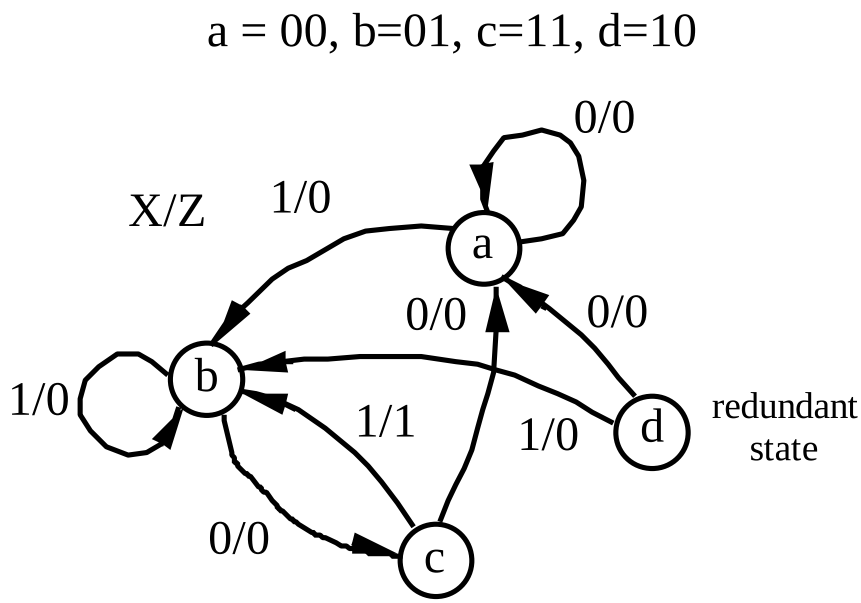
(b) What are the **next-state** and **output equations** for this machine? (9pts)

(i) Y1 = ____y1' • y2 • X'______________________

(ii) Y2 = ___X + y1' • y2______________________

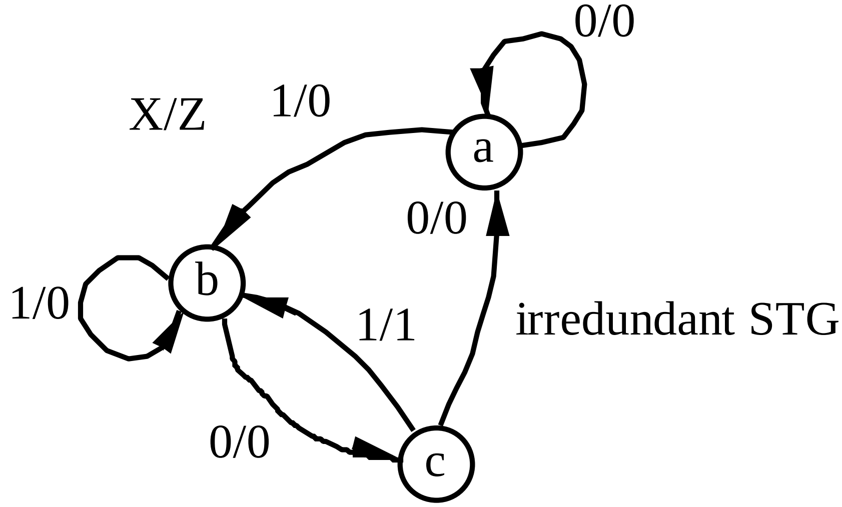
(iii) Z = ___y1 • y2 • X______________________

(c) Draw a **state transition graph (STG)** for the machine **showing all possible states and all possible transitions** (7pts)



(d) **Does the machine contain any redundant states?** If so, which state(s) are redundant and how can they be removed? **Draw an irredundant STG for the machine.** (7pts)

Yes, State d is redundant because it is identical to State a (has the same next state and outputs). By removing State d there is no change to the behavior of the machine.



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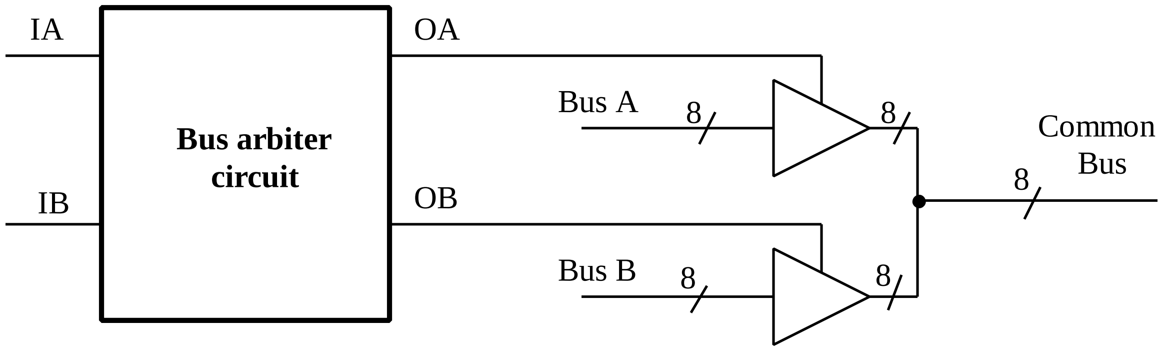
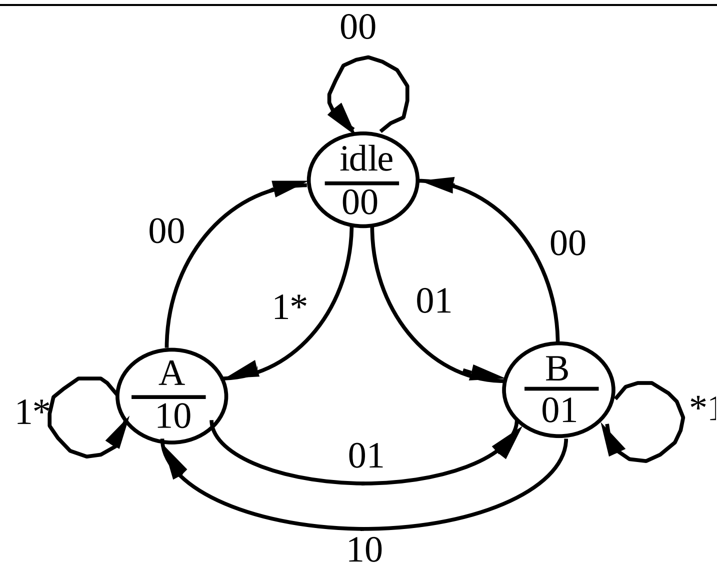
(2) You are to design a bus arbiter that operates as follows. When inputs IA IB = 0 0 the circuit either goes into the idle state (outputs OA OB = 0 0, disabling both Bus A and Bus B buffers), or remains in the idle state. When inputs IA IB change to 1 0 or 1 1 the circuit goes into State A (outputs OA OB = 1 0 enabling the Bus A buffers and disabling the Bus B buffers.) When inputs IA IB change to 0 1 while in the idle state, the circuit goes to State B (outputs OA OB = 0 1 disabling Bus A buffers and enabling Bus B buffers.) To go from State A to State B requires input IA IB = 01, and to go from State B to State A requires inputs IA IB = 1 0.



(a) Construct a **State Transition Graph** for the bus arbiter in **Moore form.** (5pts)



(b) Derive a **State Transition Table** from your graph, also in Moore form. (3pts)

	IA IB				
PS	**00**	**01**	**11**	**10**	**OAOB**
Idle	**Idle**	**B**	**A**	**A**	**00**
A	**Idle**	**B**	**A**	**A**	**10**
B	**Idle**	**B**	**B**	**A**	**01**

(c) If the idle state is encoded as Y1 Y2 = 0 0, State A is encoded as Y1 Y2 = 0 1 and State B as Y1 Y2 = 1 1, derive the **Karnaugh maps for the next-state and output functions.** (4pts)

Y1Y2 \ IAIB	00	01	11	10
Idle 00	00	11	01	01
A 01	00	11	01	01
B 11	00	11	11	01
C 10	00	xx	xx	xx

Y1n Y2n

Y1Y2 \ IAIB	00	01	11	10
Idle 00	00	00	00	00
A 01	10	10	10	10
B 11	01	01	01	01
C 10	xx	xx	xx	xx

OA OB

(d) If the machine is to be implemented using **JK flip-flops**, obtain the **Karnaugh maps for the JK flip-flop excitation inputs**. Write the **excitation input and external output equations** for the design. (10pts)

Y1Y2 \ IAIB	00	01	11	10
Idle 00	00	11	01	01
A 01	0x	1x	0x	0x
B 11	xx	xx	xx	xx
C 10	x0	xx	xx	xx

J1 J2

Y1Y2 \ IAIB	00	01	11	10
Idle 00	xx	xx	xx	xx
A 01	x1	x0	x0	x0
B 11	11	00	00	10
C 10	1x	xx	xx	xx

K1 K2

J1 = ___IA' • IB____

J2 = ___IA + IB ____

K1 = __IB' ____

K2 = __IA' • IB'____

OA= __Y1' • Y2____

OB = __Y1____

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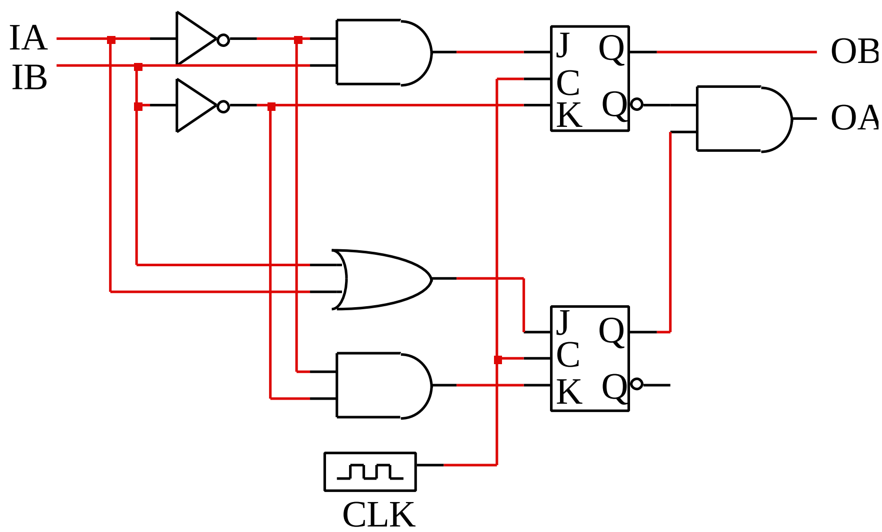
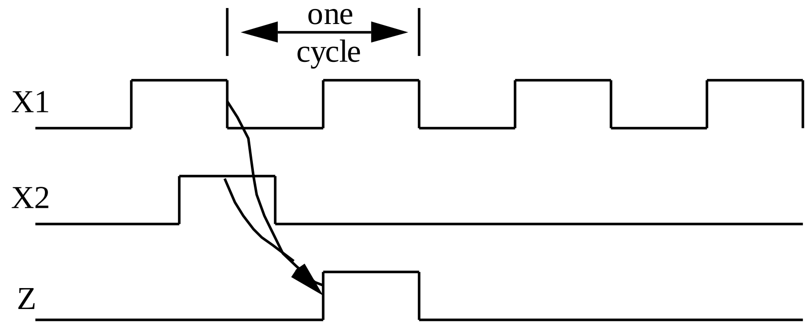
(e) Show a **schematic diagram** for the bus arbiter using **positive edge-triggered JK flop flops.** (3pts)



Extra space for Problem 2

Yin	Yi	Ji	Ki
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

(3) Design a fundamental mode asynchronous circuit with two inputs and one output. Input X1 is driven by the system clock. Input X2 is an asynchronous input. If X2 is logic 1 when X1 changes from 1 to 0, then output Z follows the waveform of input X1 for one cycle (i.e. until X1 changes again from 1 to 0.) If X2 is a logic 0 when X1 changes from 1 to 0, then Z is a logic 0 until X1 changes again from 1 to 0. Example behavior is shown in the timing diagram below. The circuit should be designed so that it is logic hazard-free, has a race-free state assignment, and can recover from illegal or unused states.



(a) Use the word description and timing diagram above to obtain a **primitive flow table** for the problem (hint: I used 7 symbolic states in Moore form) (4pts)

See labelled timing diagram on last page for state names:

PS \ X1X2	00	01	11	10	Z
a	-	-	b	a	0
b	-	c	b	-	0
c	d	c	-	-	0
d	d	-	-	e	0
e	f	-	-	e	1
f	f	-	-	g	0
g	f	-	-	g	0

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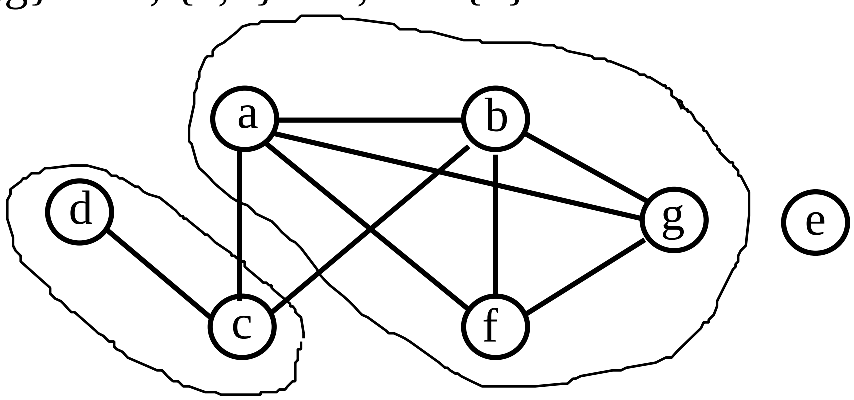
(b) Use an **implication table** to find all possible pairs of equivalent or compatible states (3pts).

	a	b	c	d	e	f
b						
c						
d	a=e					
e						
f	a=g		d=f	e=f		
g			d=f	d=f e=g		

(c) Construct a **merger diagram** from the results of (b) and **list the sets of mergeable states that will lead to the minimum number of states** for the design. (3pts)

merge {a,b,f,g} to H, {c,d} to I, and {e} to J



(d) Obtain a **reduced flow table** from the above, giving a **unique state name to each group of states merged** into a single state (hint: I ended up with 3 merged states, in Moore form). (3pts)

PS \ X1X2	00	01	11	10	Z
H	H	I	H	H	0
I	I	I	-	J	0
J	H	-	-	J	1

(e) Examine the reduced flow table and **add additional states if necessary to obtain a critical-race-free state assignment** for the circuit. (hint: requires two state bits) (3pts)

H = {00}, I = {01}, J = {11}, must add K = {10} for J-H transition.

(f) Construct a composite **Karnaugh map for the next-state and external output logic functions** from your state assignment. (3pts)

PS \ X1X2		00	01	11	10	Z
H	00	00	01	00	00	0
I	01	01	01	-	11	0
J	11	10	-	-	11	1
K	10	00	01	00	00	-

Y1n Y2n

(g) Modify your combinational logic, if necessary, to **eliminate hazards** from the design. State what you are doing and why you are doing it. (2pts)

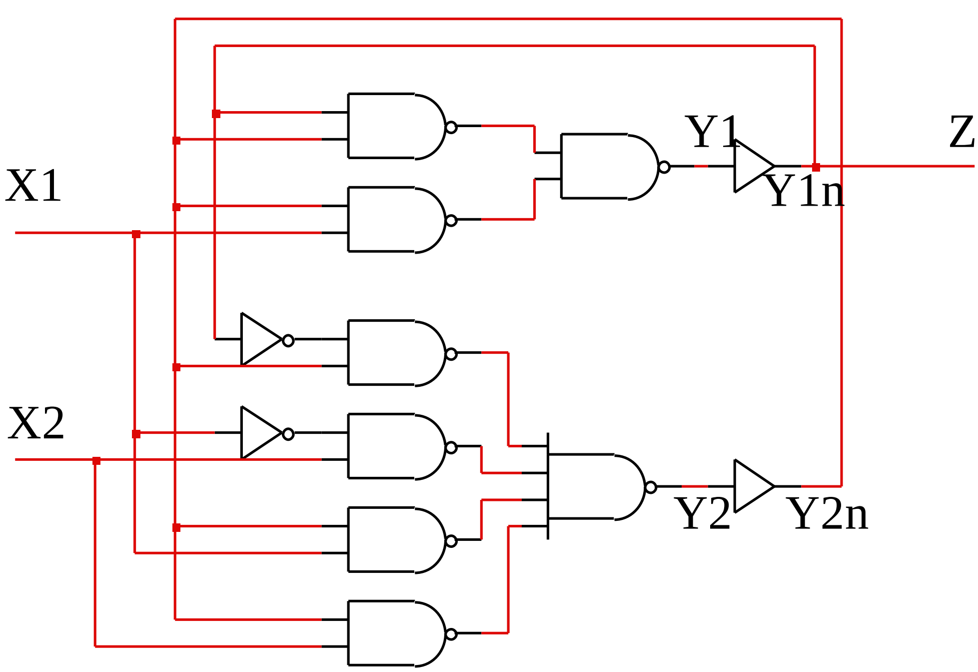
By linking all terms in the Karnaugh map, we eliminate hazards and equations become:

Y1n = Y1•Y2 + Y2•X1

Y2n = Y1'•Y2 + X1'•X2 + Y2•X1 + Y2•X2

Z = Y1

(h) Draw a **gate-level asynchronous sequential circuit diagram** for the design. Represent the asynchronous delay element(s) in feedback loops with a buffer symbol. (4pts)



Additional space for Problem 3