Your Name: _____

UNIVERSITY OF CALIFORNIA AT BERKELEY

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SANTA BARBARA • SANTA CRUZ

Department of Electrical Engineering
and Computer Sciences

CS 150 - Spring 1990
Prof. A. R. Newton

Quiz 1

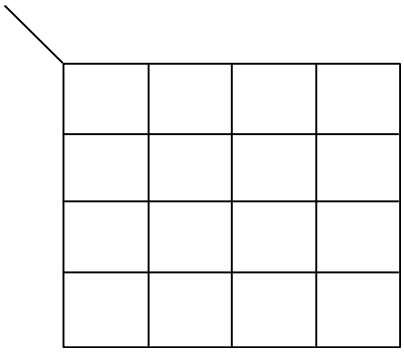
Room 22 Warren, Tuesday 2/20
(Open Wakerly, Calculators OK, 1hr 40min)

Include all final answers in locations indicated on these pages. Use reverse side of sheets for all working. If necessary, attach additional sheets by staple at the end. BE SURE TO WRITE YOUR NAME ON EVERY SHEET. Postulates & Theorems are summarized on page 10 for your convenience.

(1) Given the following function:

$$f(A,B,C,D) = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,C\,\overline{D} + A\overline{B}\,C\,D + ABCD + A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}\,\overline{C}\,D + A\overline{B}\,CD + A\overline{B}\,C\,\overline{D}$$

(a) Show a Karnaugh Map representation:



(b) Determine:
(i) The **Standard** Sum-of-Products form:

f(A,B,C,D) =

(ii) The **Standard** Product-of-Sums form:

f(A,B,C,D) =

(c) Determine:
(i) The **simplest** Sum-of-Products form:

f(A,B,C,D) =

(ii) The **simplest** Product-of-Sums form:

f(A,B,C,D) =

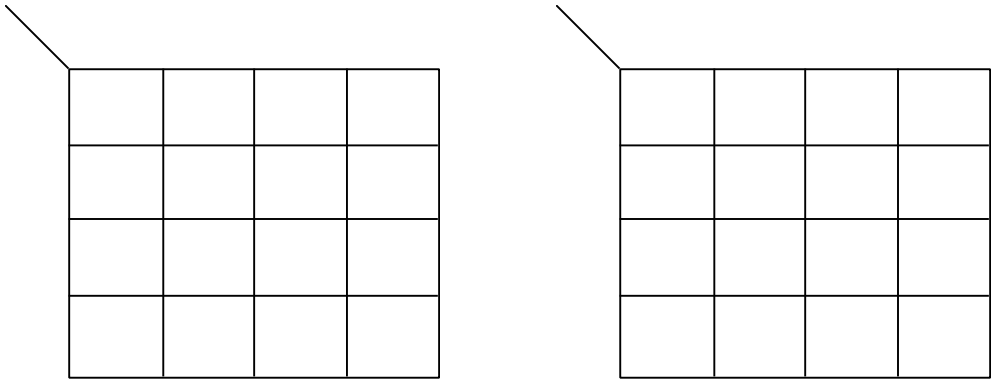
(d) Draw a schematic diagram for the simplest Sum-of-Products form. Assume complements are **not** available.

(working space for Problem 1)

Your Name: _____

(2) Four people judge a competition. The vote of each is indicated by a 1 (pass) or 0 (fail) on an input wire. The four wire form the inputs to a logic circuit. The rules of the competition allow one dissenting vote. If the vote is 2-2 (a tie), then the competition must continue. The logic circuit is to have two outputs, x and y. If the vote is 4-0 or 3-1 to pass, then x=y=1. If the vote is 4-0 or 3-1 to fail, then x=y=0. If the vote is 2-2, then x=1 and y=0.

(a) Show Karnaugh Maps for outputs x and y.

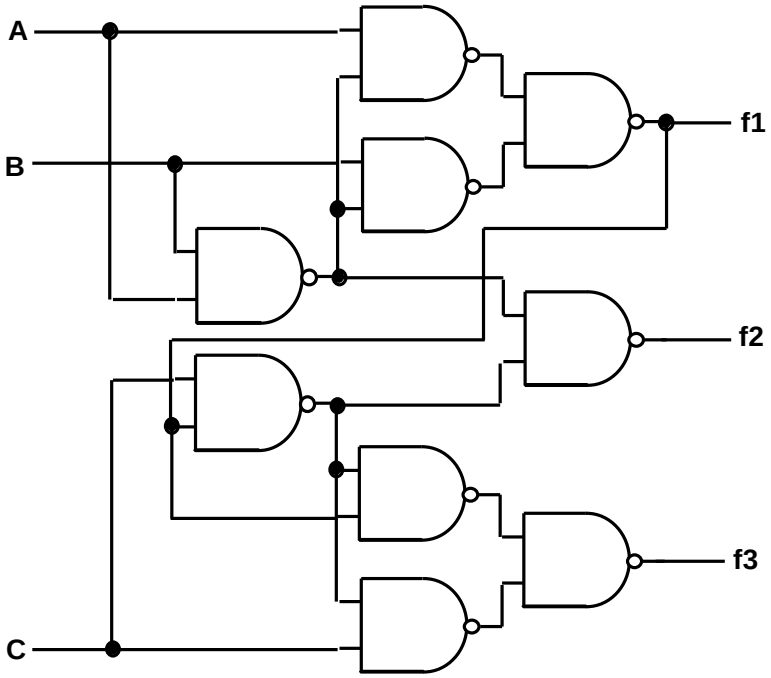


(b) Realize the logic using a minimum number of logic gates. Assume complements are available.

(working space for Problem 2)

Your Name: _____

(3) Consider the following schematic diagram:



(a) Develop expressions for f1, f2, and f3 as functions of A, B, and C.

f1 =

f2 =

f3 =

(b) Develop a minimum implementation (use any type of logic gates) for f3. Show a schematic diagram.

(working space for Problem 3)

Your Name: _____

(4) (a) Use two-input NAND gates to convert a positive-edge-triggered T flip-flop with enable to a J-K flip-flop.

(b) Does your logic include a hazard? Explain why or why not. If it does contain a hazard, show how it can be removed.

(working space for Problem 4)

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Summary of Laws and Theorems of Boolean Algebra

Identities:	(T1)	X + 0 = X	(T1')	X•1 = X
Null Elements:	(T2)	X + 1 = 1	(T2')	X•0 = 0
Indempotency:	(T3)	X + X = X	(T3')	X•X = X
Involution :	(T4)	(X')' = X		
Complements:	(T5)	X + X' = 1	(T5')	X•X' = 0
Commutativity:	(T6)	X + Y = Y + X	(T6')	X•Y = Y•X
Associativity:	(T7)	(X+Y)+Z = X+(Y+Z)	(T7')	(X•Y)•Z = X•(Y•Z)
Distributivity:	(T8)	X•Y+X•Z = X•(Y+Z)	(T8')	(X+Y)•(X+Z) = X+Y•Z
Covering:	(T9)	X + X•Y = X	(T9')	X•(X+Y) = X
Combining:	(T10)	X•Y + X•Y' = X	(T10')	(X+Y)•(X+Y') = X
Consensus:	(T11)	X•Y+X'•Z+Y•Z = X•Y+X'•Z		
	(T11')	(X+Y)•(X'+Z)•(Y+Z) = (X+Y)•(X'+Z)		
DeMorgan:	(T13)	(X•Y•Z)' = X'+Y'+Z'	(T13')	(X+Y+Z)' = X'•Y'•Z'
Shannon:	(T15)	F(X,Y,Z) = X•F(1,Y,Z) + X'•F(0,Y,Z)		

(T15') F(X,Y,Z) = (X+F(0,Y,Z))•(X'+F(1,Y,Z))

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(additional working space)