

EECS150 Name \_\_\_\_\_  
 Midterm2  
 3/23/06 SID \_\_\_\_\_

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2	/15
3	/20
4	/15
5	/20
6	/10
7	/15
Total	/

1. (5 points)

a. In an 8 bit 2s complement number system, what is the representation of -3? -127?

b. Using a standard 4 bit 2s complement representation, write down 3-5 and solve.

c. What are the most positive and most negative numbers that can be represented in a 12 bit 2s complement system, and what are their binary representations?

2. (15) Your friend is designing a custom chip with an 8 bit adder. He only needs to represent a few small negative numbers, and sometimes needs to represent numbers a little larger than 127. He decides to change the normal 2s complement representation and allocate  $\frac{1}{4}$  of the wheel to negative numbers and  $\frac{3}{4}$  to positive numbers. He does this by defining that numbers with both b7 and b6 equal to 1 are negative, and all other numbers are positive. The remaining negative numbers are still represented as in normal 2s complement: -1 is still  $8'b11111111$  and so on.

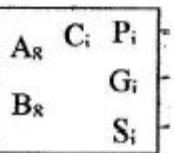
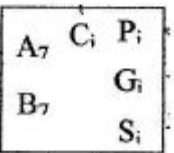
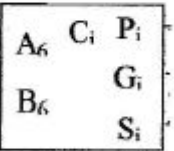
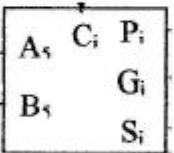
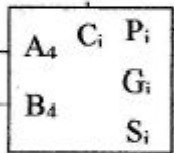
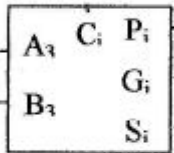
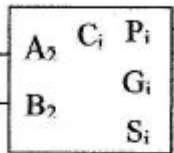
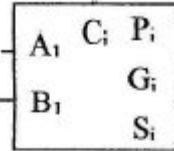
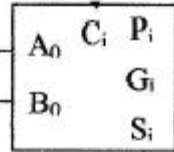
a. What is the range of positive and negative numbers that he can represent?

b. Is it possible for the sum of one positive and one negative number to overflow in this number system?

- c. (Prob 2 cont.) Given two negative numbers, implement an overflow detector for detecting when their sum overflows. Use only inverters, AND, and OR gates. You don't need to check that the two numbers are negative.
- d. Given two positive numbers, implement an overflow detector for detecting when the sum of two positive numbers overflows. Use only inverters, AND, and OR gates. You don't need to check that the two numbers are positive.

3. (20) In this problem you will design a 9 bit carry lookahead adder:
- a. Using inverters and AND and OR gates with arbitrary numbers of inputs, design a 3 bit carry lookahead generator. Assume that single bits generate P and G terms as normal. Your lookahead generator should have inputs  $P_i$  and  $G_i$  for  $i=0,1,2$ , and generate  $C_1$ ,  $C_2$ , and the group  $P_{2:0}$  and group  $G_{2:0}$  terms.

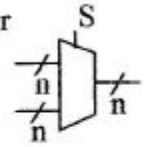
- b. Carefully draw all of the connections for a hierarchical 9 bit adder using your carry lookahead parts, and label all of the outputs of your lookahead parts and all sums with their signal delays.



4. (15) You have implemented an 8 bit ripple carry adder block on an FPGA and measured its worst-case delay at 1ns. You have 2-to-1 MUXes with a delay of 0.1ns.

a. Carefully draw a 32 bit carry-select adder using only your 8 bit ripple carry adder and 2-to-1 MUXes as building blocks.

b. What is the worst case delay through your adder?



c. If the delay in your ripple-carry adder is linear in the number of bits, what is the fastest combination of ripple and carry select to implement a 32 bit adder? (i.e. should you use a 4 bit ripple carry adder and more muxes? A 16 bit ripple and fewer muxes?). How many bits in each ripple carry adder, and how many layers of muxes would you use? What would the final worst-case delay be? \_\_

5. (20) Design a 4 bit ripple-carry ALU which implements the following function: When  $M=0$  (arithmetic) And when  $M=1$  (logic)

S1	S0	F
0	0	A
0	1	A+1
1	0	A+B
1	1	A-B

S1	S0	F
0	0	A NOR B
0	1	$\neg A$ NOR $\neg B$
1	0	B
1	1	$\neg B$

Draw the whole ALU carefully first, and then show the details of the bit slices. You may use inverters, AND, OR, XOR, and MUXes with arbitrary number of inputs.

6. (10) In the following circuit, the 8x3 bit SRAM starts with all zeros stored in its memory. The counter is enabled and counts normally. Assume that the clock period is long compared to any SRAM timing constraints. What is the contents of the memory after a few dozen clock ticks? Does it ever change after that?

