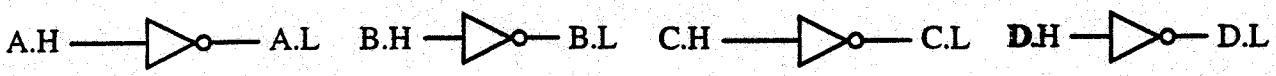
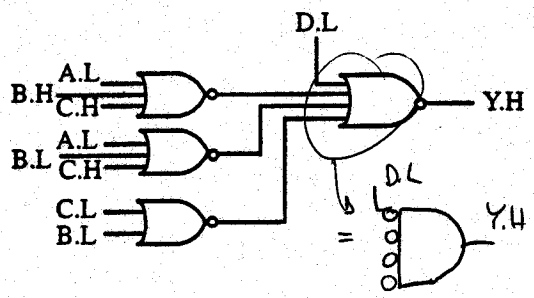
Problem 1 (15 points) KEY

[8 pts.] **a)** You are given the logic diagram below. Complete the truth table for Y.H = f(A, B, C, D). Hint: Bubble matching and simplify.



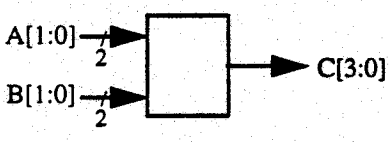


$Y = D \cdot (\bar{C} + \bar{B})(\bar{A} + B + C)(A + \bar{B} + C)$

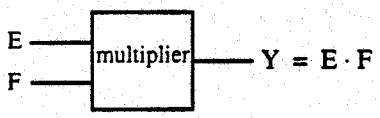
D	C	B	A	Y = f(A, B, C, D)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0

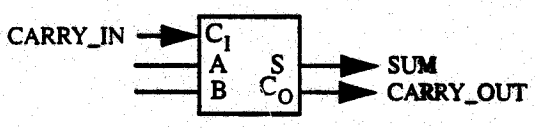
D	C	B	A	Y = f(A, B, C, D)
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

[7 pts.] **b)** In this problem you will design a combinational circuit that outputs C[3:0], which is the product of two 2-bit binary numbers A[1:0] and B[1:0], as shown in the block diagram below.



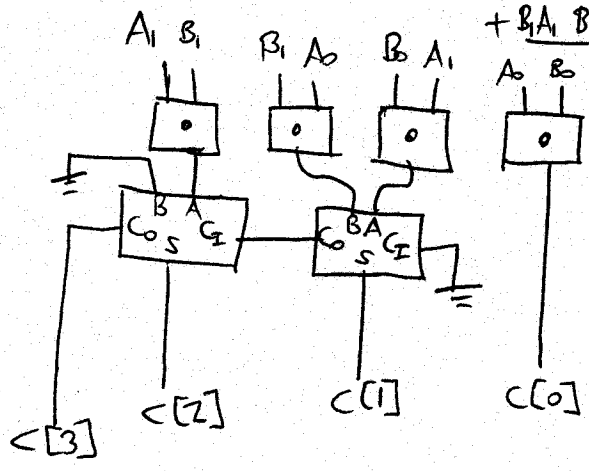
The multiplier is built from an appropriate interconnection of 1-bit multipliers and 1 bit full adders:





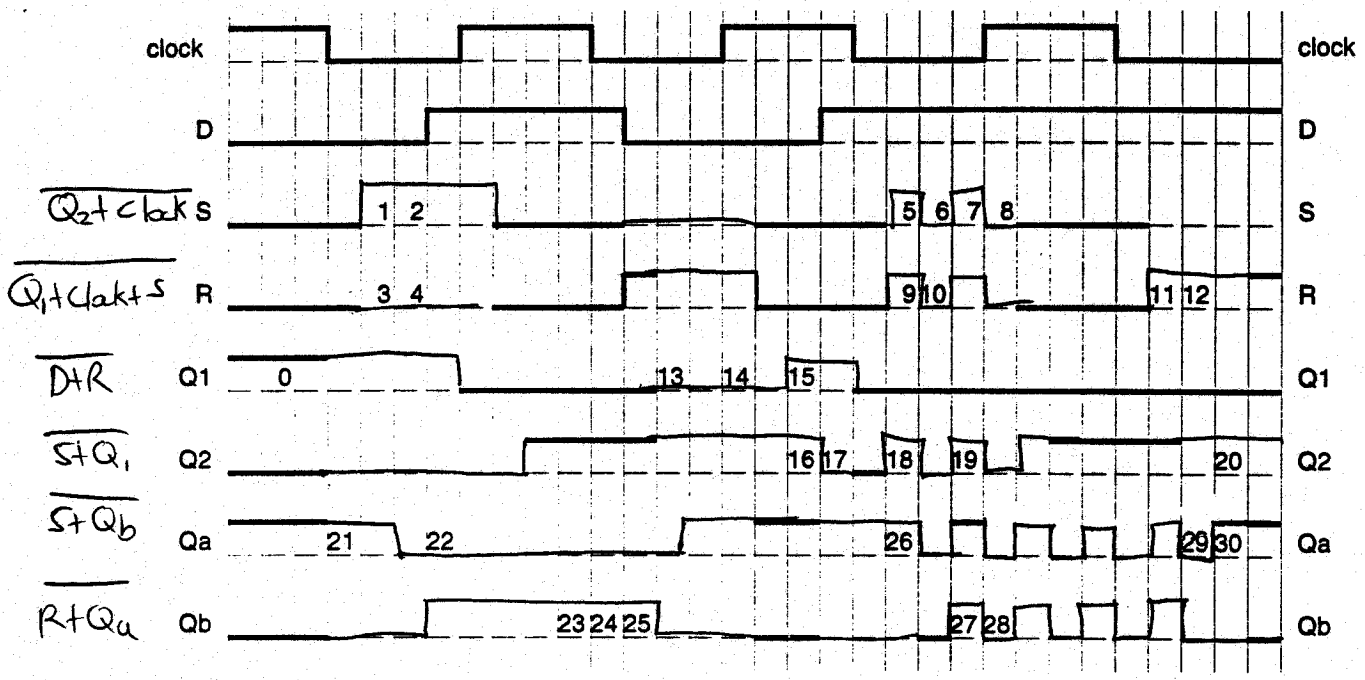
Show how the 1-bit multiplier and full adder modules would be interconnected, using only wires, but no extra gates or inverters.

$A_1\ A_0$
$\times\ B_1\ B_0$
$B_0A_1\ B_0A_0$
$+ B_1A_1\ B_1A_0$

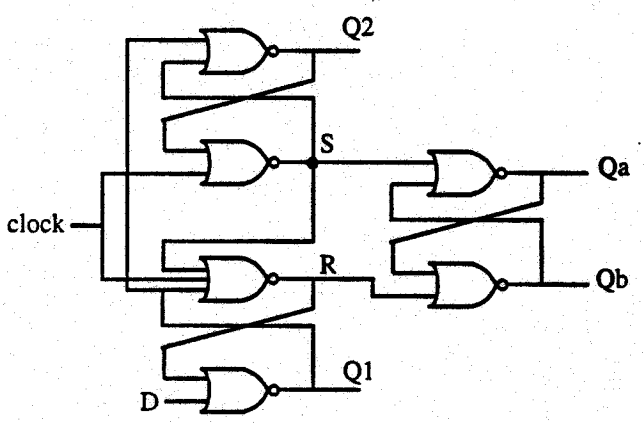


Problem 2 (30 points) KEY

Complete the timing diagram for the figure below, assuming unit delays for all gates and inverters (transport delay only), and no delay in the wires. (The dashed lines in the diagram represent missing sections of the timing diagram.) Complete the table below with the voltage levels at the specified location in the timing diagram, i.e., **L** for low and **H** for high. Example: At location 0, the appropriate *voltage* level is H. (This problem will be graded +1 for correct, 0 for blank, and −1 for incorrect, with minimum score of 0 points.)

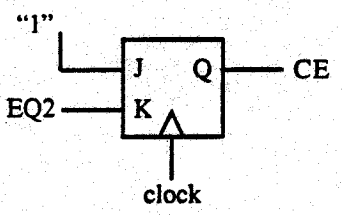


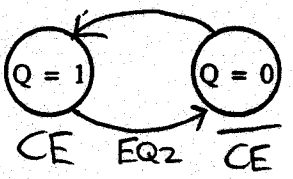
1	H	6	L	11	H	16	H	21	H	26	H
2	H	7	H	12	H	17	L	22	L	27	H
3	L	8	L	13	L	18	H	23	H	28	L
4	L	9	H	14	L	19	H	24	H	29	L
5	H	10	L	15	H	20	H	25	H	30	H



Problem 3 (15 points) FSM Analysis KEY

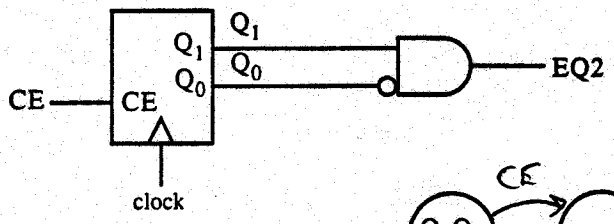
[2 pts.] **a)** Complete the state diagram for the following FSM, independently of part b):

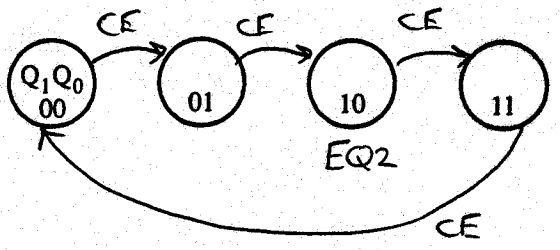




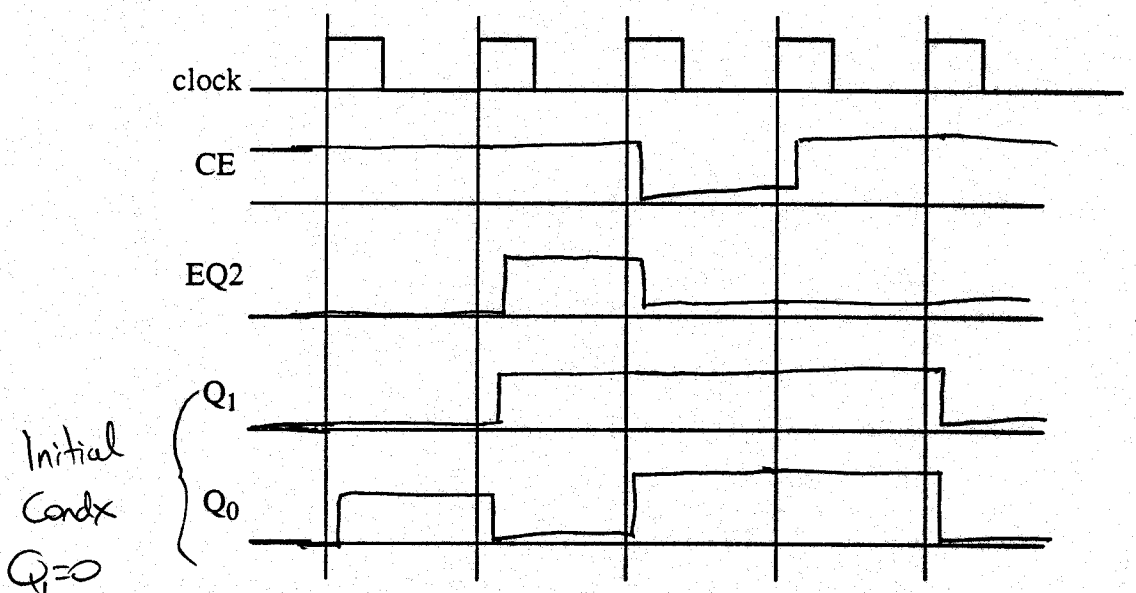
JK	Q^+
00	Q_n
01	0
10	1
11	$\overline{Q_n}$

[3 pts.] **b)** Complete the state diagram for the following 2-bit binary up counter FSM, independently of part a):





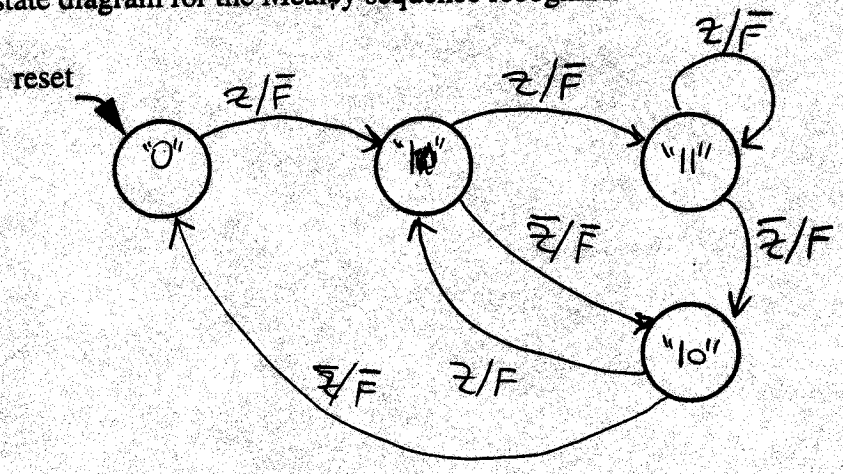
[10 pts.] **c)** Draw a functional timing diagram for the two FSMs above connected together with common clock, CE(a) tied to CE(b), and EQ2(a) tied to EQ2(b).



Problem 4 (?? points) KEY

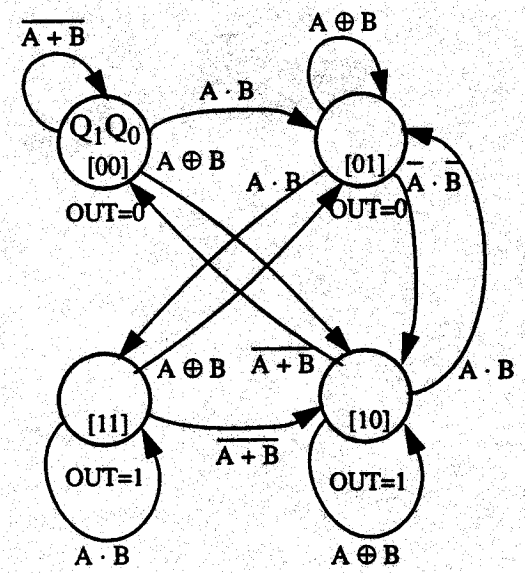
[0 pts.] a) Design a state diagram for a Mealey FSM with synchronized input Z.H and output F.H, which recognizes possibly over-lapping patterns of 101 or 110. For example, if Z= 101101, then output F = 001011.

Complete the state diagram for the Mealey sequence recognizer:



Problem 5 (?? points) KEY

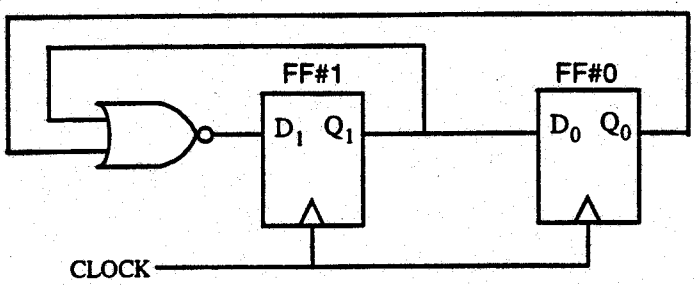
You are given the following state diagram:



Complete the state table for this state diagram.

Present State Q_1	Q_0	Inputs A	B	Next State Q_1	Q0	Output OUT
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	1	0
0	1	1	1	1	1	0
1	0	0	0	0	0	1
1	0	0	1	1	0	1
1	0	1	0	1	0	1
1	0	1	1	0	1	1
1	1	0	0	1	0	1
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	1	1	1

Problem 6 (20 points) KEY

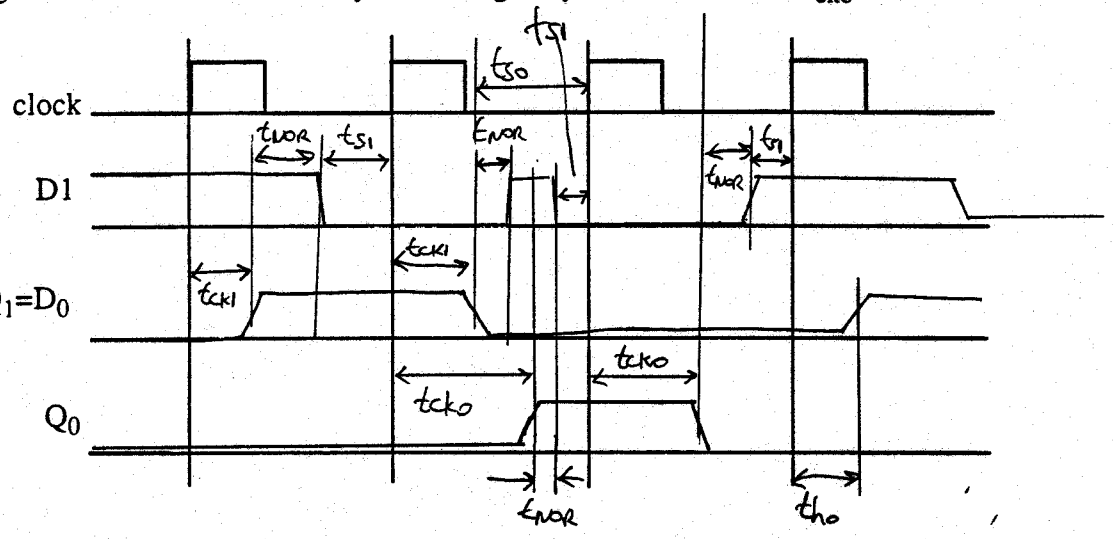


Data:	FF #1	FF #0
hold time	$t_{h1} = 4$ ns	$t_{h0} = 8$ ns
setup time	$t_{s1} = 10$ ns	$t_{s0} = 20$ ns
propagation delay through FF	$5 < t_{ck1} < 9$ ns	$10 < t_{ck0} < 18$ ns

propagation delay through NOR: $7 < t_{NOR} < 12$

[14 pts.] a) Complete a detailed timing diagram (assuming maximum delays) for the FSM above using given timing data. Show all critical delays, labelling in symbolic form, i.e., t_{cko} not 18 ns.

note:
$t_{ck1max} > t_{ho}$ by assumption of maximum delay, so FSM could work.



[3 pts.] b) What is the minimum clock period (assuming maximum delays) for proper operation of this FSM?

$\max\{t_{ck1}+t_{NOR}+t_{s1},\ t_{cko}+t_{NOR}+t_{s1},\ t_{ck1}+t_{s0}\} = \max\{9+12+10,\ 18+12+6,\ 9+20\} = \max\{31,40,24\}$

40ns

[3 pts.] c) If the clock period = 1000 ns, will this FSM operate correctly? Why or why not?

No. Possible hold time violation on FF#0.

$t_{ck1\,min} = 5\text{ns} < t_{ho} = 8\text{ns}$